Ultra Low Spur 4-Bit SP4T Tuning Switch 1 MHz to 3.0 GHz

Features

- $R_{DS\text{-}ON}$ 1.1 Ω
- C_{OFF} 0.21 pF
- RF peak voltage handling of 100 V
- 4-bit control, 16 possible independent state configurations
- No external DC blocking capacitors on RF lines
- DC supply: V_{DD} 2.6 V – 5.5 V and V_{CP} −18 V
- 1.2 V – 5.0 V GPIO compatible control bus
- Ultra low spur operation, charge pump disabled, requires −18 V external supply

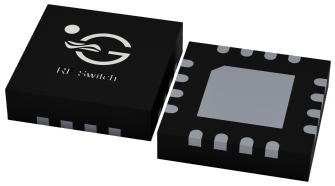

Figure 1: TS63421K in 3.0 x 3.0 mm^2 QFN 16-pin package.

Applications

- Tunable RF filters, dynamic matching, and antenna tuning
- Private mobile radio handsets
- Public safety handsets
- Cellular infrastructure and satellite terminals
- Biomedical instruments and implant device charging

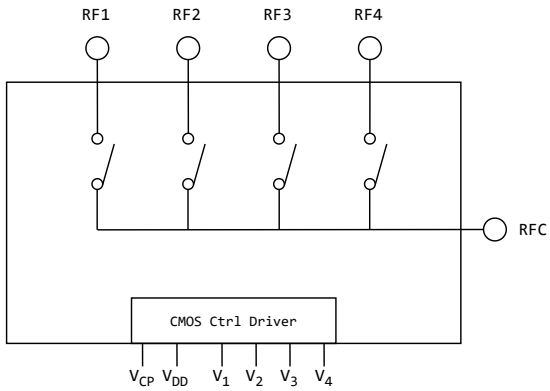

Figure 2: TS63421K functional diagram [top view]

General Description

The TS63421K is a reflective open Single Pole Four Throw (SP4T) switch designed for antenna and filter tuning applications where high RF peak voltage handling is desired. The TS63421K is suitable for the frequency range from 1 MHz to 3.0 GHz. The TS63421K has a very low 1.1 Ω on-resistance and an off capacitance of 0.21 pF. The switch can select up to 16 independent states through its 4-bit control bus. The internal charge pump has been disabled to eliminate the charge pump spurs; a clean −18 V DC supply is needed on the V_{CP} pin to achieve ultra low spurs.

The TS63421K is housed in a compact 3.0×3.0 mm^2 16-lead Quad Flat No-lead (QFN) plastic package.

RoHS

RoHS10/REACH/Halogen free

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Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TS63421K	16 Pin 3.0x3.0x0.75 mm^3 QFN	Core part number
TS63421K-EVB	Evaluation Board	
TS63421KMTRPBF[1]	330 mm reel, 3 000 pcs	Full reel

[1] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	13” (330mm)	18mm

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Pin Assignment

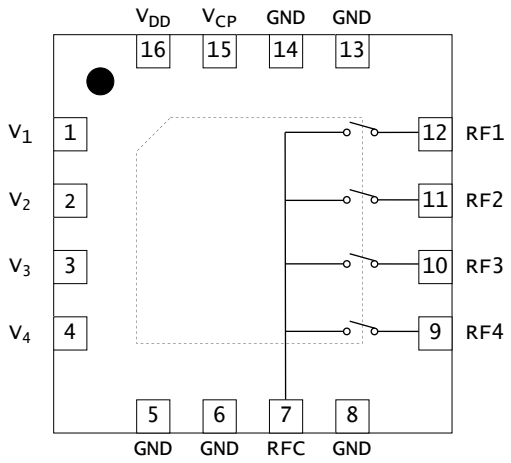

Figure 3: TS63421K pin assignment and functional diagram [top view]

Table 3: Pin Definition

Pin Number	Pin Name	Description
1	V_1	Switch control input 1
2	V_2	Switch control input 2
3	V_3	Switch control input 3
4	V_4	Switch control input 4
5, 6, 8, 13, 14	GND	No internal connection, should be grounded
7	RFC	RFC (Antenna) port
9	RF4	RF port 4
10	RF3	RF port 3
11	RF2	RF port 2
12	RF1	RF port 1
15	V_{CP}	Negative voltage supply, -18 V[2]. Connect a 1nF capacitor to GND on this pin.
16	V_{DD}	DC Power Supply, add a 10nF bypass capacitor to GND close to this pin.
17 [1]	GND	Ground thermal pad, please connect to GND

[1] The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

[2] V_{DD} must be applied first, before the external -18 V is applied to V_{CP}. Shutdown should be done in the reverse order.

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	V_{DD}	6	V
External bias voltage on V_{CP} pin	V_{CP}	-20	V
Storage Temperature Range	T_{st}	−55 – 125	°C
Operating Temperature Range	T_{op}	−40 – 85	°C
Maximum Junction Temperature	T_j	+140	°C
Maximum RF CW input power, 800 MHz	RFx	41	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	20	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta jt}$	$\leq$39	°C/W
Soldering Temperature	T_{solder}	+260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 – $<$1000	V
Charged Device Model (CDM)	Level C3	$\geq$1000	V
Moisture Rating			
Moisture Sensitivity Level[2]	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and can cause permanent damage to the device. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.

[2] Tagore recommends to store parts in moisture barrier bag to preserve solderability.

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Electrical Specifications

Table 5: Electrical Specifications $T_A = +25°C; V_{DD} = +2.7V; V_{CP} = -18V$ (external supply); 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	1		3000	MHz
ON resistance	On state, DC measurement		1.1		Ω
OFF capacitance	Total capacitance of each OFF path		0.21		pF
RF peak voltage	Measured at 10 MHz		100		V
Insertion loss	100MHz		0.25		dB
$ANT - RFx$	500MHz		0.40		dB
	1.0GHz		0.45		dB
	2.0GHz		0.85		dB
	3.0GHz		1.4		dB
Isolation	100MHz		40		dB
$ANT - RFx$	500MHz		26		dB
	1.0GHz		20		dB
	2.0GHz		15		dB
	3.0GHz		12		dB
Return loss	100MHz		-43		dB
$ANT - RFx$	500MHz		-31		dB
	1.0GHz		-22		dB
	2.0GHz		-15		dB
	3.0GHz		-11		dB

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Table 6: Electrical Specifications $T_A = +25°C; V_{DD} = +2.7V; V_{CP} = -18V$ (external supply); 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	1		3000	MHz
Harmonic Distortion					
H_2	800MHz, P_{in} =35dBm		-91		dBc
H_3	800MHz, P_{in} =35dBm		-102		dBc
IIP3	800MHz		71		dBm
Power and Compression point					
$P_{0.1dB}$[1]	1 – 10MHz		40		dBm
$P_{0.1dB}$[1]	10 – 1000MHz		42		dBm
Switching Time					
t_{SW}[3]	Switching time, $C_{VCP} = 1nF$		2.0		μs
$t_{startup}$[4]	Start-up time, $C_{VCP} = 1nF$		TBD		μs
Power Supply, DC					
Control voltage	Power Supply V_{DD}	2.6	2.7	5.5	V
	Charge pump supply[6], V_{CP}	-19	-18	-15	V
	All control pins high[5], V_{ih}	1.0	2.7	5.25	V
	All control pins low, V_{il}	-0.3	0	0.5	V
Control current	All control pins high, I_{ih}			7.5	μA
	All control pins low, I_{il}		0		μA
Current consumption	I_{DD}, active mode (V_{DD} on)		50	80	μA
	I_{CP}, active mode, current on V_{CP}		100		μA

[1] $P_{0.1\,dB}$ is a figure of merit. Please do not exceed Absolute Maximum ratings.
[2] No external DC blocking capacitors are required on the RF pins unless a DC voltage is applied on a RF pin.
[3] From 50% of the control signal to 10/90% of the settled RF value. $C_{VCP} = 1nF$ to GND on the V_{CP} pin.
[4] Start-up time is the time from V_{DD} ON to the RF signal settled on a throw, or the transition time from low power mode to active mode.
[5] Control voltage V_{ih} cannot be higher than V_{DD} (to avoid forward biasing of ESD diode)
[6] V_{DD} must be applied first, before the external -18 V is applied to V_{CP}. Shutdown should be done in the reverse order.

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Switch Truth Table

Table 7: Switch Truth Table with V_{DD}

V_{DD}[1]	V_1	V_2	V_3	V_4	**Active RF Path**
1	x[2]	x	x	1	RF4 ON
1	x	x	1	x	RF3 ON
1	x	1	x	x	RF2 ON
1	1	x	x	x	RF1 ON
1	0	0	0	0	All OFF state
0	0	0	0	0	All ON state[3]
1	1	1	1	1	All ON state

[1] V_{DD} should be applied first before V_1, V_2, V_3 and V_4, otherwise may cause damage to the device.
[2] x = don't care.
[3] When V_{DD} is 0 V, all switch FETs are on regardless of the control inputs, i.e. every RF path is conducting (All ON state). Do not apply voltage to control inputs.
[4] If there is no DC path to ground on the ANT-to-RF port paths, the switch will not change its state. See Standard Tuning Switch Configurations for more details.
[5] There are internal pull-downs to ground on all control pins; the state at start-up without any control voltage applied will be All OFF.

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Internal Circuit Model

A simplified equivalent circuit model of the TS63421K is shown below, together with the model component values.

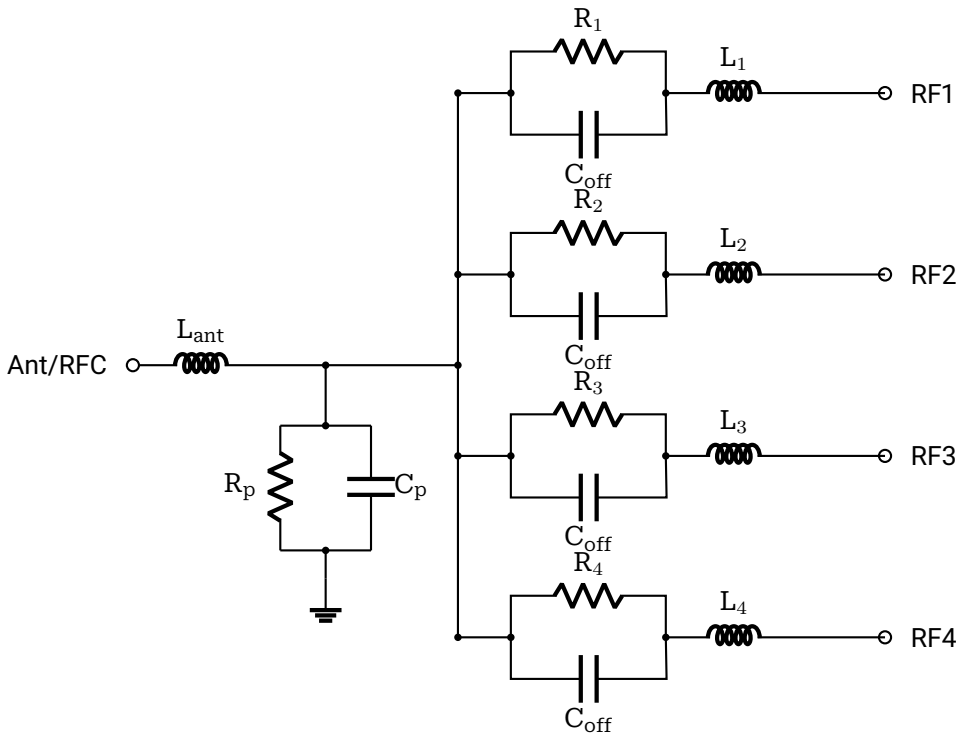

Figure 4: Equivalent circuit model.

Table 8: Simplified equivalent circuit model component values

Component	Value	Unit
R_p	12.5k	Ω
C_p	0.95	pF
C_{off}	0.21	pF
$R_1 - R_4$	1.1 if ON state 78k if OFF state	Ω Ω
L_{ant}	0.9	nH
$L_1 - L_4$	0.6	nH

Note: $R_{ON/OFF}$ is measured at DC. The circuit model is a general purpose model and will not accurately predict full performance, such as Q and losses in a tunable filter or antenna design. For more accuracy, it is recommended to use the customized s-parameter model, which is available for download: Download TS63421K s-parameter model

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SP4T tuning switch simulation model

- Derived 5-port touchstone s-parameter model files
- 16 total .S5P files for all 4-bit state combinations
- Frequency range up to 3 GHz
- Accurately predicts Q and losses
- Compatible with ADS/Microwave Office
- EM simulation of the PCB is recommended
- Accurate models of external components, such as inductors and capacitors, are required

Table 9: Port definitions in the s-parameter model files.

PIN name	Port number	Function
RF1	1	RF port 1
RF2	2	RF port 2
RF3	3	RF port 3
RF4	4	RF port 4
ANT	5	Antenna port (Ant/RFC)

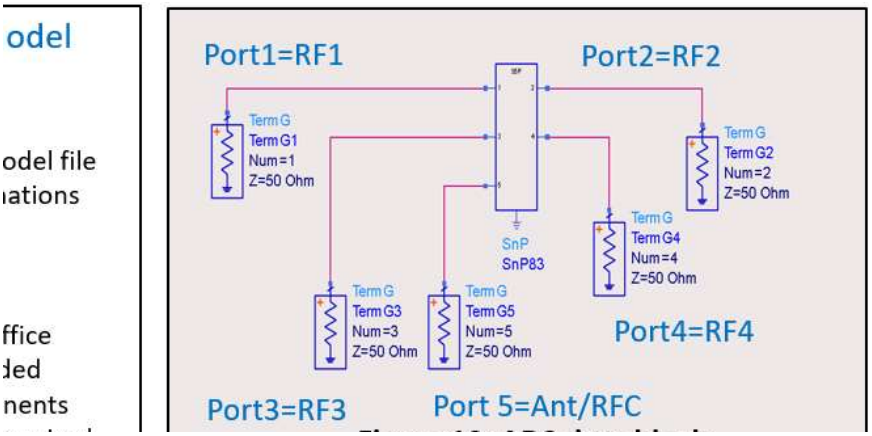

Figure 5: ADS data block of the 5-port s-parameter model.

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Standard Tuning Switch Configurations

Series Configuration

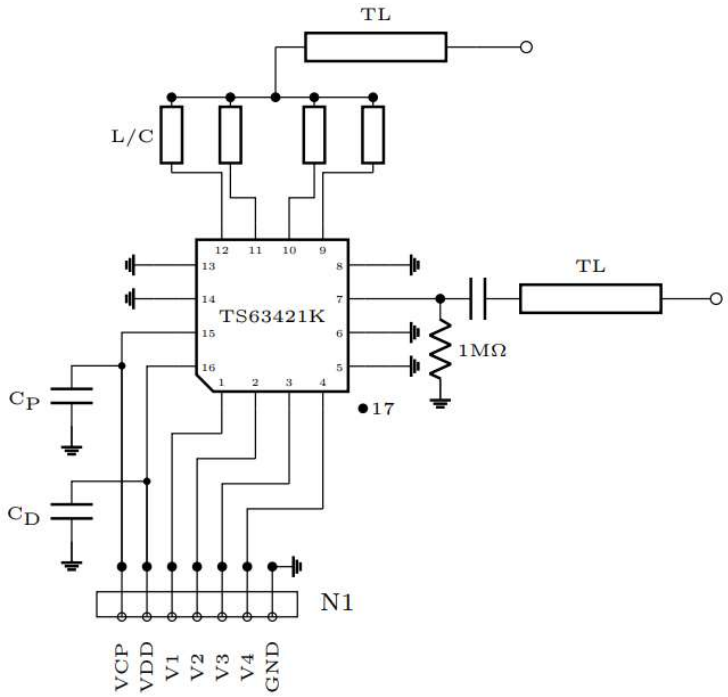

Figure 6: Series configuration. DC reference required.

Note: Series configurations require a DC path, since all RF and ANT ports are AC coupled. The DC reference can be provided through a 1 MΩ resistor, as shown in Figure 6.

Shunt Configuration

Note: Shunt configurations do not require a DC path to ground, since the ANT port is DC grounded, as shown in Figure 7.

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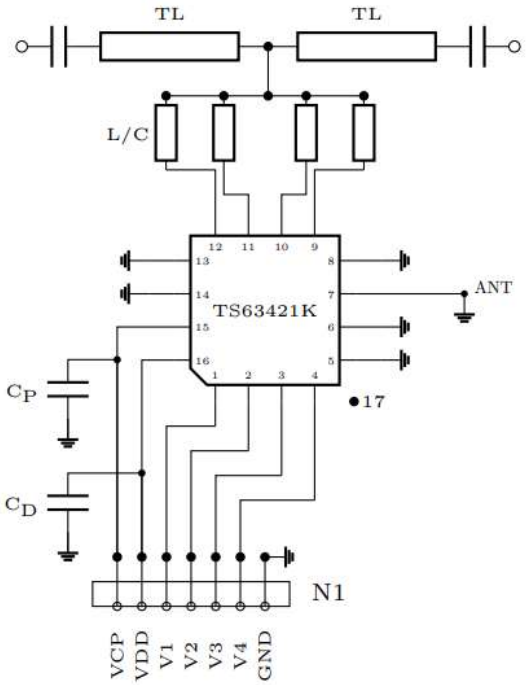

Figure 7: Shunt configuration. No DC reference required.

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Schematics and Evaluation Board

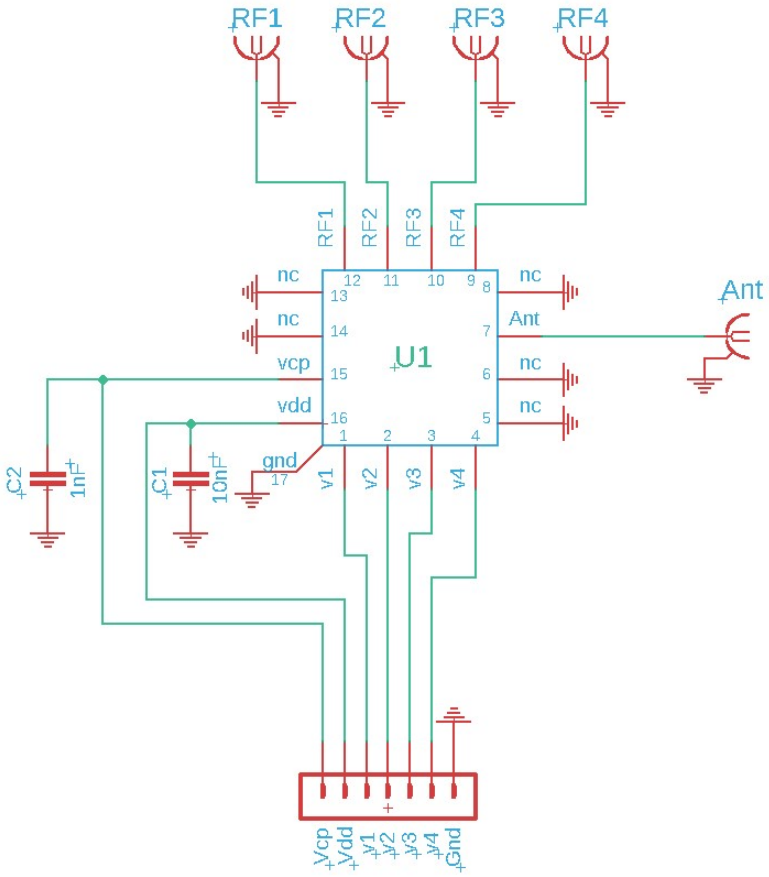

Figure 8: Evaluation board schematic.

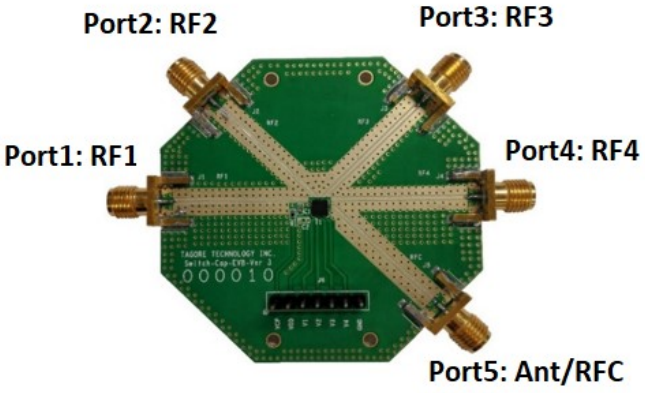

Figure 9: Evaluation board. Port1: RF1, Port2: RF2, Port3: RF3, Port4: RF4, Port5: Ant/RFC.

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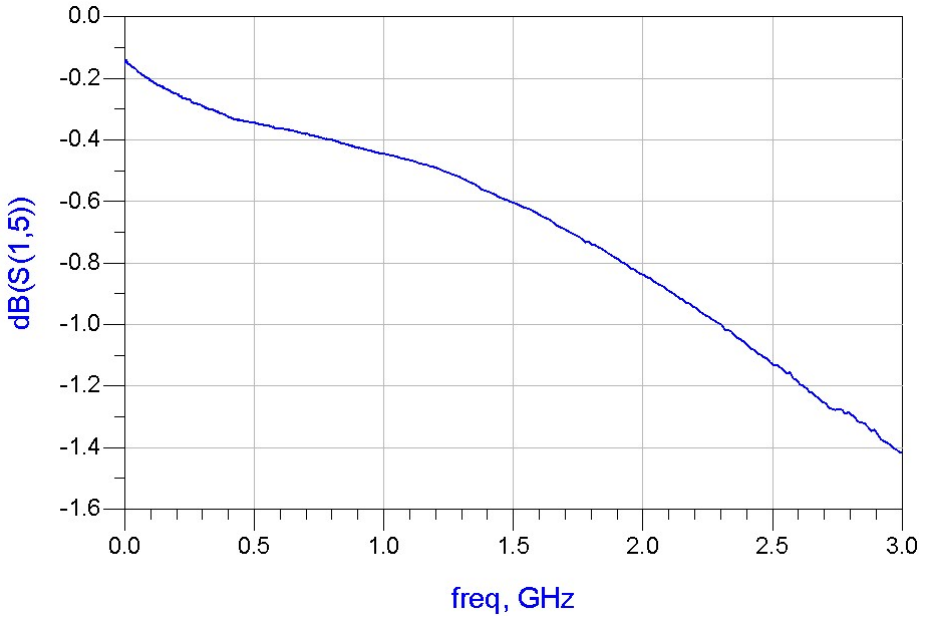
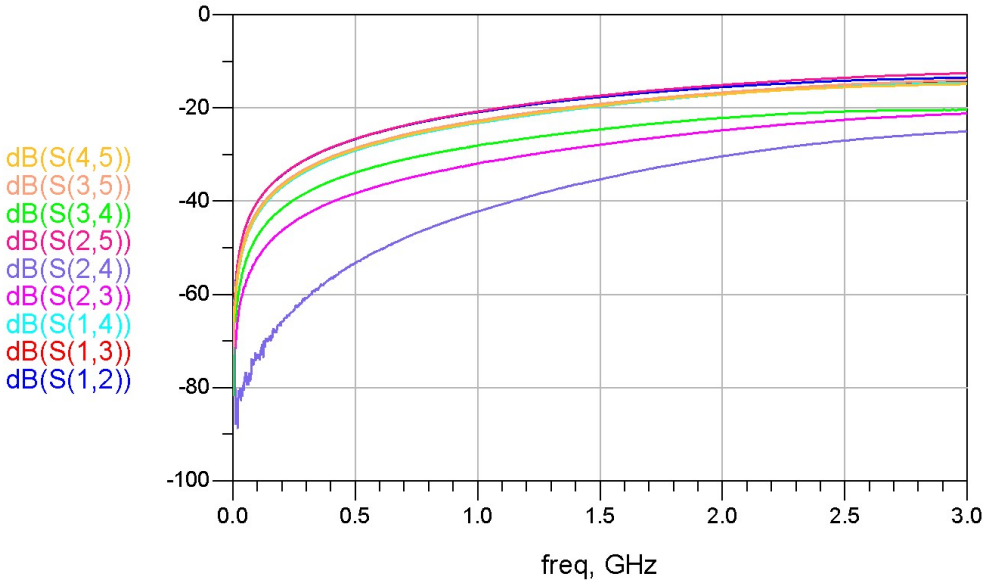
Typical characteristics

The following measurements were obtained from the TS63421K evaluation board.



Insertion loss between RF1 – Ant for RF1-On state 0001.



All port-to-port isolations for RF1-On state 0001.

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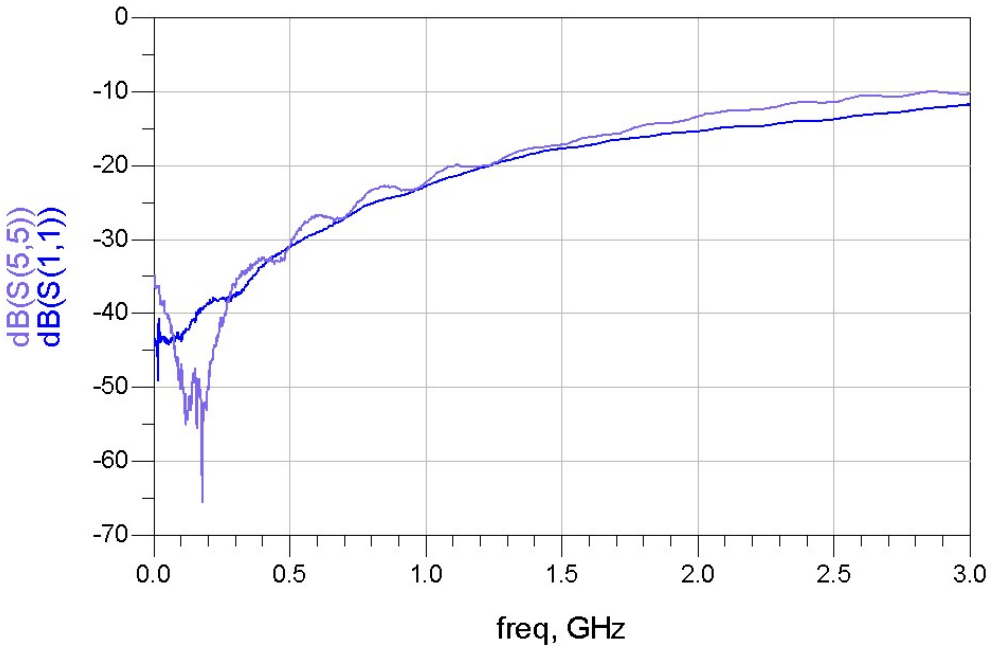
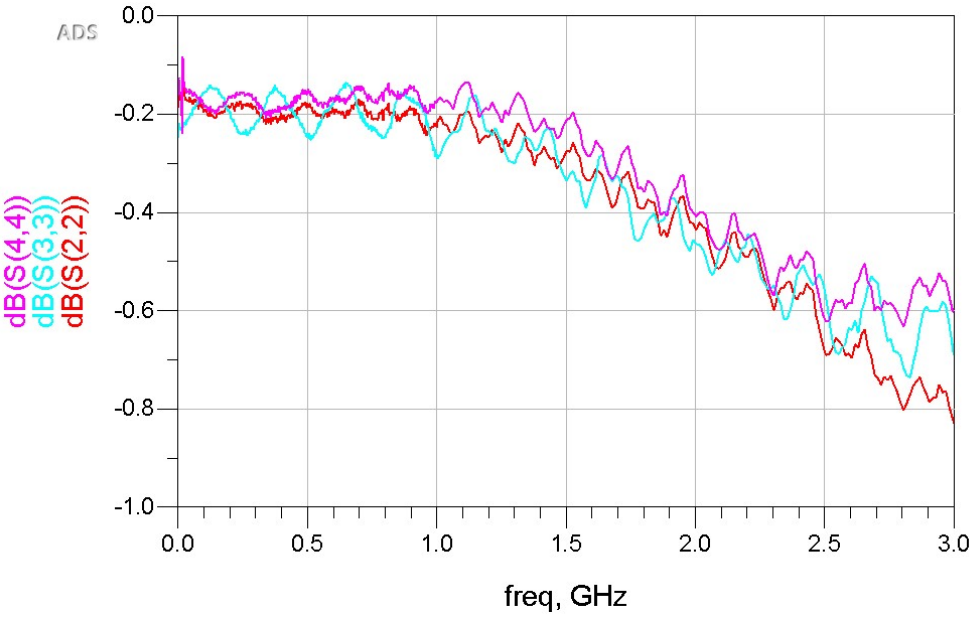


On-port return loss for RF1 and Ant port for RF1-On state 0001.



Off-port return loss for RF1-On state 0001.

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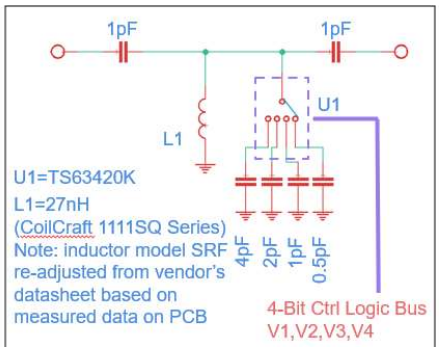
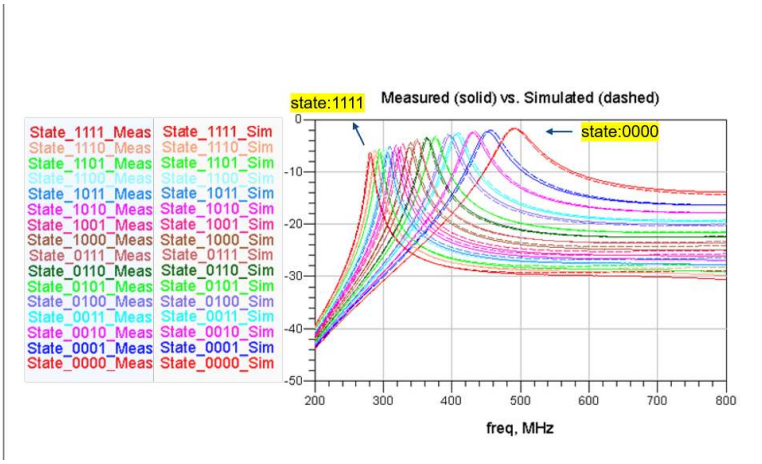
Application Board Examples

Application Board 1: Tunable band-pass filter 280 – 500 MHz (1 switch, 1-pole LC resonator)



(a) Schematic.



(b) Measured (solid) vs. simulated (dashed) filter response.

Figure 10: Tunable band-pass filter, 280 – 500 MHz.

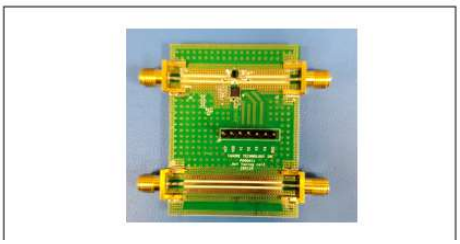


Figure 11: Application board 1.

Note: The simulation was performed using the s-parameter model (not the circuit model), see Internal Circuit Model.

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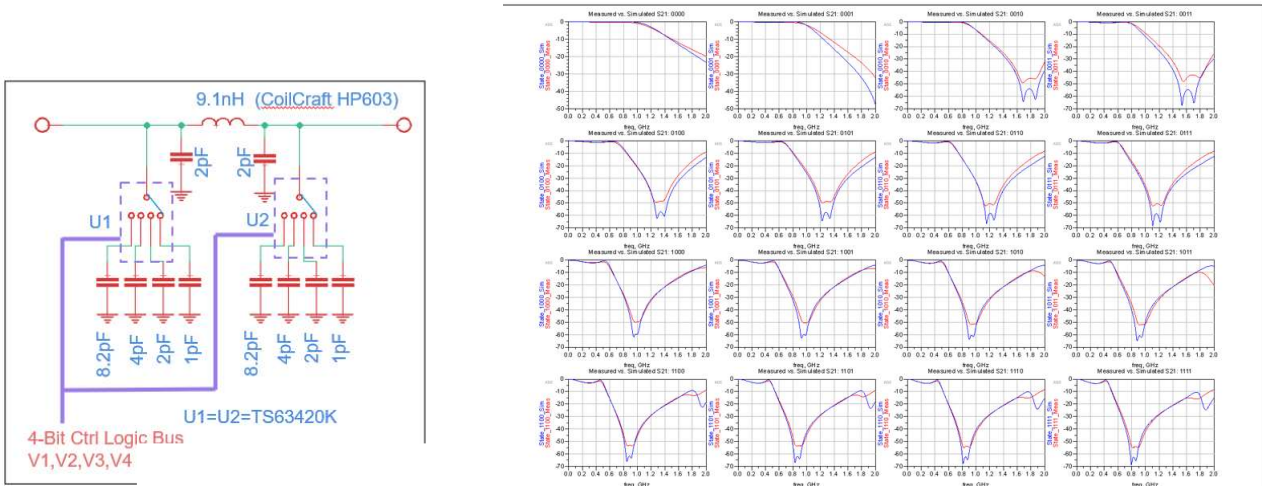
Application Board 2: Tunable low-pass filter 500 – 1000 MHz (2 switches, 3-element Pi-network)



(a) Schematic.

(b) Measured (blue) vs. simulated (red) filter response for all 16 states.

Figure 12: Tunable low-pass filter, 500 – 1000 MHz.

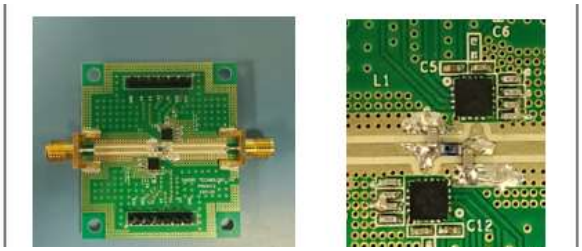


Figure 13: Application board 2.

Note: The simulation was performed using the s-parameter model (not the circuit model), see Internal Circuit Model.

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Device Package information

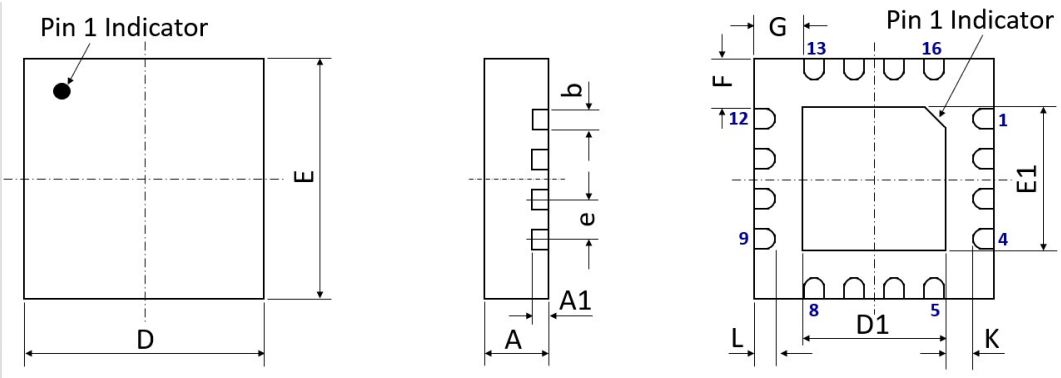

Figure 14: 16-pin QFN 3.0 x 3.0 x 0.75 mm^3 package drawing.

Please refer to application notes TN-001 PCB Design guideline and TN-002 Solder Rework at TagoreTech web page for PCB and soldering guidelines.

Table 10: Device Package Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A	0.75	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm – 20μm (Typical 10μm – 12μm).

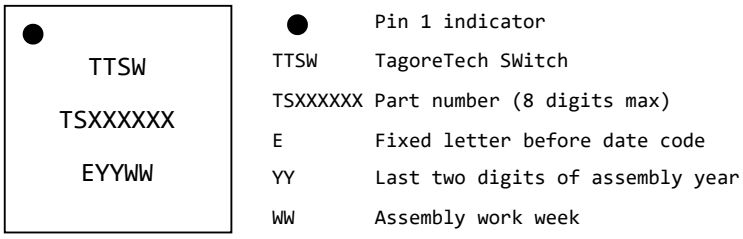

Figure 15: Part marking specification.

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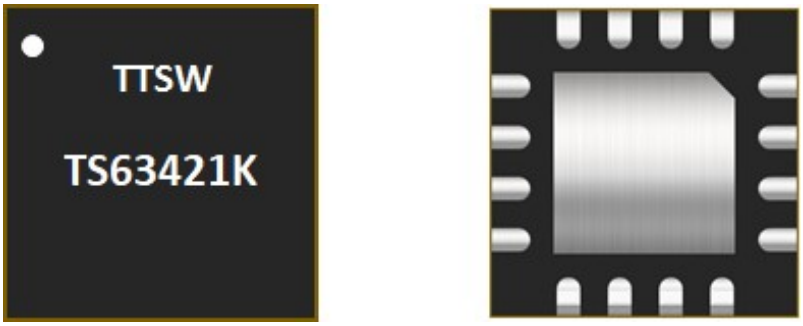

Figure 16: TS63421K photo, top side and package bottom.

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PCB Land Design

Notes:

- 4-layer PCB is recommended.
- Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
- Thermal vias shall only be placed on the center pad.
- The maximum via number for the center pad is 3(X)×3(Y)=9.

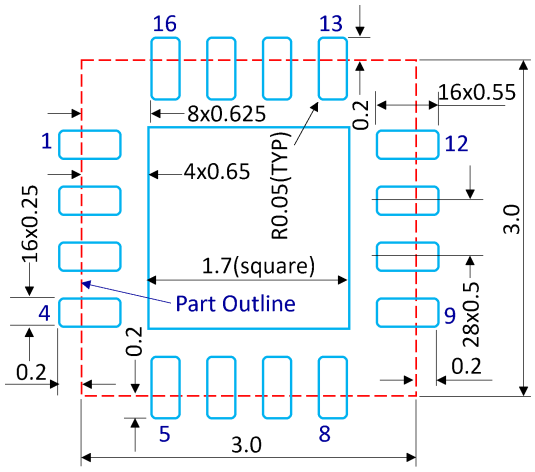

Figure 17: PCB land pattern, dimensions in [mm].

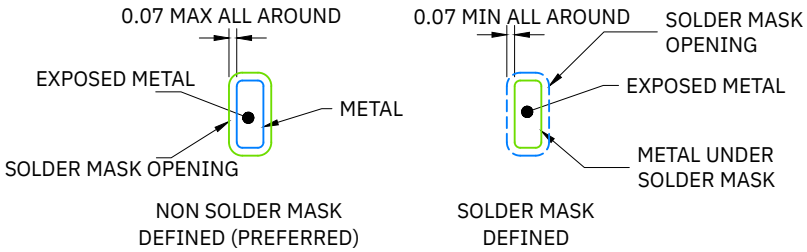

Figure 18: Solder mask opening, dimensions in [mm].

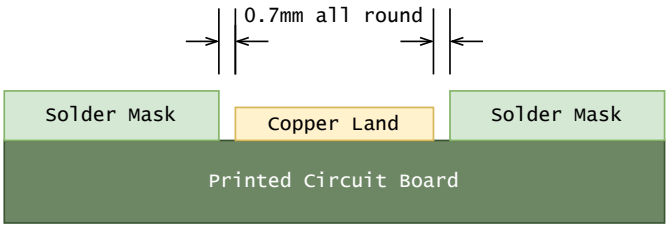

Figure 19: Preferred solder mask opening, side view, dimensions in [mm].

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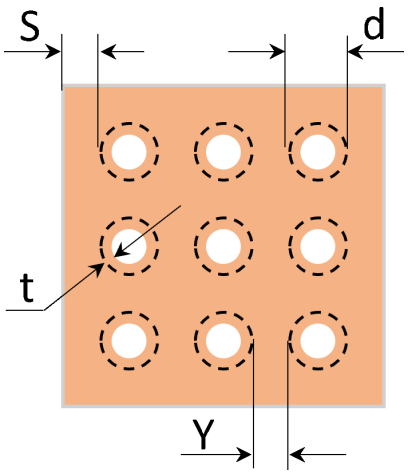

Figure 20: Thermal Via Pattern, Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm.

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PCB Stencil Design

Notes:

- Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- Stencil thickness is recommended to be 125μm.

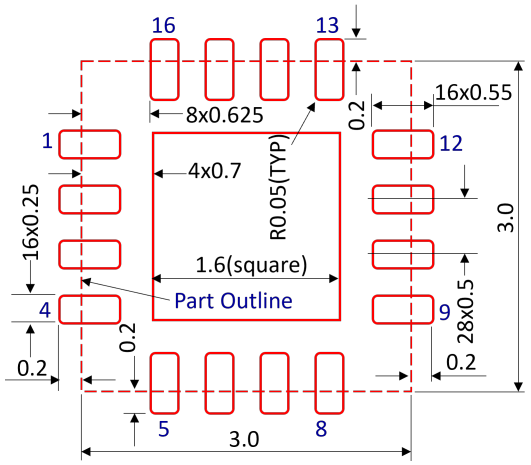

Figure 21: Stencil Openings, dimensions in [mm].

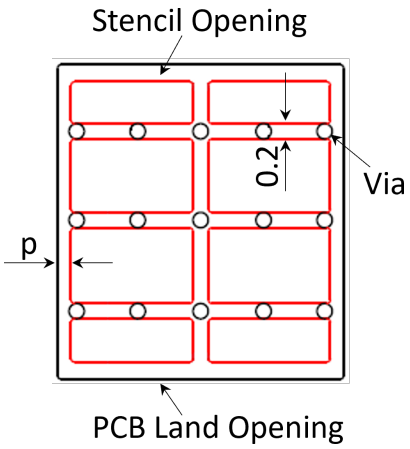

Figure 22: Stencil Openings Shall not Cover Via Areas If Possible, dimensions in [mm].

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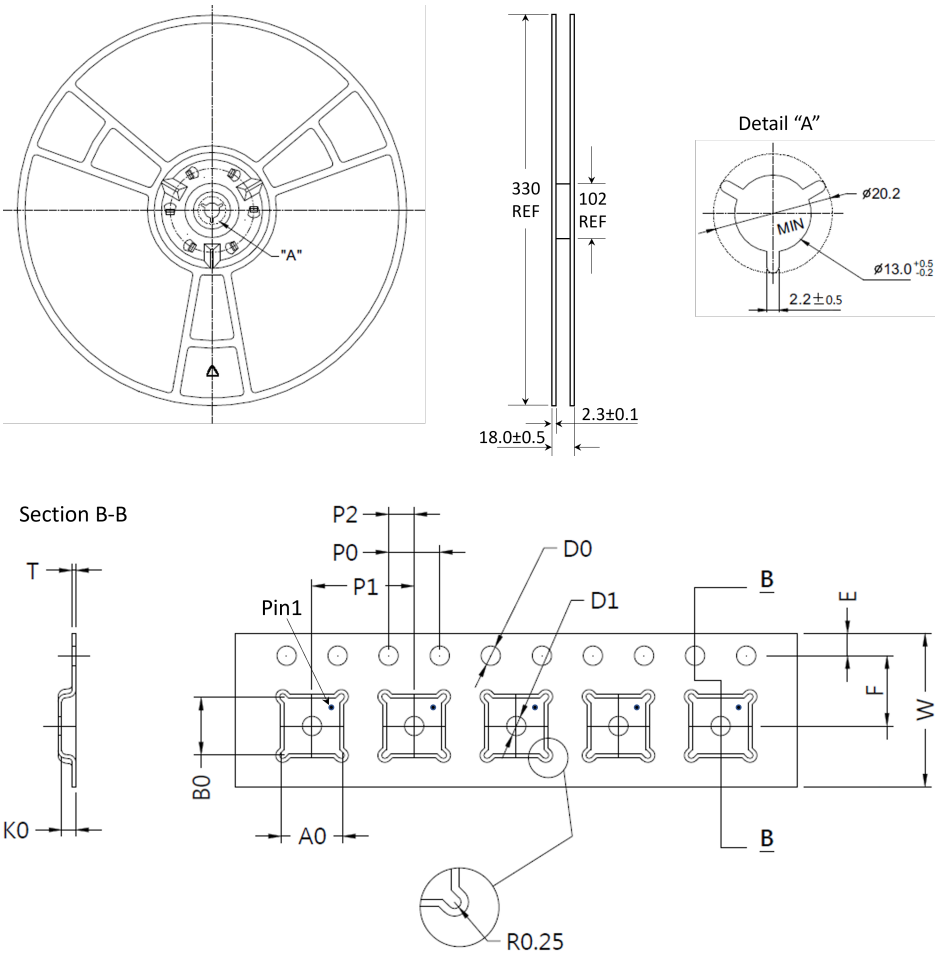
Tape and Reel Information



A0[mm]	B0[mm]	D0[mm]	D1[mm]	E[mm]	F[mm]	K0[mm]	P0[mm]	P1[mm]	P2[mm]	T[mm]	W[mm]
3.35	3.35	1.50	1.50	1.75	5.50	1.10	4.00	8.00	2.00	0.30	12.00

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Glossary

C_{OFF}	Off capacitance of an RF path
IL	Insertion loss
ISO	Isolation
$R_{DS\text{-}ON}$	On resistance of an RF path
RL	Return loss
SP4T	Single Pole Four Throw
VSWR	Voltage Standing Wave Ratio
ANT	Antenna port, sometimes referred as RFC (RF Common)
RFx	RF Port number x

Changelog

Table 11: Changelog

Date	Revision	Notes
08/23/2024	2.0	Datasheet in the previous format.
09/25/2026	3.00	Datasheet converted to common TagoreTech document template: QR code link to the latest datasheet, links to application notes TN-001/TN-002, package height corrected to 0.75mm, V_{CP} absolute maximum rating of -20V, return loss and harmonics given in house sign convention, V_{CP} supply sequencing note added.

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