SP2T 1.1 Ω GaN Tuning Switch 1 MHz to 3 GHz

Features

- Frequency Range 1 MHz to 3 GHz
- Low 1.1 Ω ON resistance
- Low 0.28 pF OFF capacitance
- RF peak voltage handling of 120 V
- Each throw can be controlled independently
- 4 independent state configurations
- No external DC blocking capacitors on RF lines
- Versatile 2.6 V – 5.5 V power supply
- 1.2 V – 5.0 V digital control

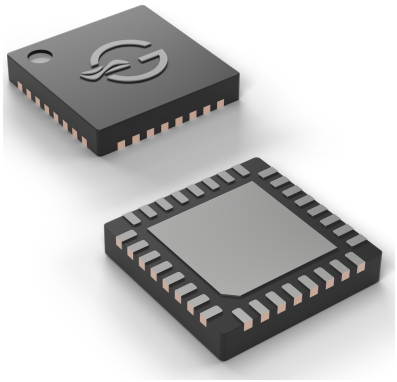

Figure 1: TS64210L in 4.0 x 4.0 mm^2 QFN 32-pin package.

Applications

- Filter and antenna tuning
- Dynamic matching
- Private mobile radio handsets
- Public safety handsets

General Description

The TS64210L is a reflective open Single Pole Two Throw (SP2T) switch designed for antenna or filter tuning applications where high RF peak voltage handling is desired. The TS64210L is suitable for the frequency range from 1 MHz to 3 GHz. The TS64210L has a low 1.1 Ω ON resistance and an OFF capacitance of 0.28 pF. Both throws are controlled independently, so the switch can select up to 4 independent states.

The TS64210L is housed in a compact 4.0×4.0 mm^2 32-lead Quad Flat No-lead (QFN) plastic package.

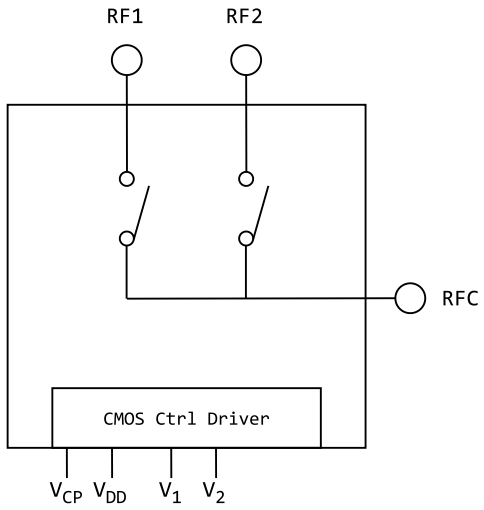

Figure 2: TS64210L functional diagram

RoHS10/REACH/Halogen free

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Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TS64210L	32-Pin 4.0x4.0x0.75 mm^3 QFN	Core part number
TS64210L-EVB	Evaluation Board	
TS64210LMTRPBF[1]	330 mm reel, 3 000 pcs	Full reel

[1] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	13” (330mm)	18mm

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Pin Assignment

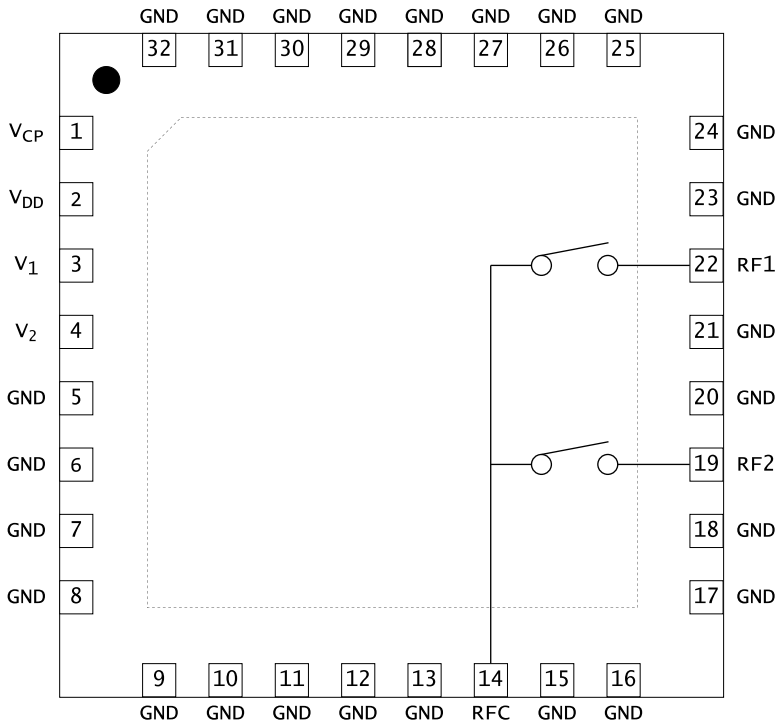

Figure 3: TS64210L pin assignment [top view]

Table 3: Pin Definition

Pin Number	Pin Name	Description
1	V_{CP}	Internal charge pump voltage output. Connect a 1 nF capacitor to GND on this pin to improve switching time.
2	V_{DD}	DC Power Supply
3	V_1	Switch control input 1 ($RFC - RF1$)
4	V_2	Switch control input 2 ($RFC - RF2$)
14	RFC	RF common port (antenna port)
19	RF2	RF port 2
22	RF1	RF port 1
5–13, 15–18, 20, 21, 23–32	GND	No internal connection, connect to ground[2]
33 [1]	GND	Ground thermal pad, please connect to GND

[1] The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.

[2] These pins are NC pins inside the package. To avoid floating pins around RF lines, we request these to be connected to ground.

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	V_{DD}	5.5	V
External bias voltage on V_{CP} pin	V_{CP}	-20	V
Storage Temperature Range	T_{st}	−55 – 125	°C
Operating Temperature Range	T_{op}	−40 – 85	°C
Maximum Junction Temperature	T_j	+140	°C
Maximum RF CW input power, 800 MHz	RFx	42	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	10	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta jt}$	$\leq$25	°C/W
Soldering Temperature	T_{solder}	+260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 – $<$1000	V
Charged Device Model (CDM)	Level C3	$\geq$1000	V
Moisture Rating			
Moisture Sensitivity Level[2]	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and can cause permanent damage to the device. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.

[2] Tagore recommends to store parts in moisture barrier bag to preserve solderability.

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Electrical Specifications

Table 5: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	1		3000	MHz
ON resistance, R_{ON}	ON state, DC measurement		1.1		Ω
OFF capacitance, C_{OFF}	Total capacitance of each OFF path		0.28		pF
RF peak voltage	Measured at 10 MHz		120		V
Insertion loss	100 MHz		0.13		dB
RFC – RFx	500 MHz		0.17		dB
	1.0 GHz		0.24		dB
Isolation	100 MHz		40		dB
RFC – RFx	500 MHz		26		dB
	1.0 GHz		21		dB
Return loss	100 MHz		-35		dB
RFC – RFx	500 MHz		-32		dB
	1.0 GHz		-30		dB

Table 6: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Linearity					
H_2	800 MHz, P_{in} =45 dBm		-86		dBc
H_3	800 MHz, P_{in} =45 dBm		-79		dBc
IIP3	800 MHz		75		dBm
Power and Compression point					
$P_{0.1dB}$[1]	1 to 10 MHz		43		dBm
$P_{0.1dB}$[1]	10 to 1000 MHz		46		dBm
Switching Time					
t_{SW}[2]	Switching time, $C_{VCP} = 1$ nF		4.0		μs
$t_{startup}$[3]	Start-up time, $C_{VCP} = 1$ nF		TBD		
Power Supply, DC					
Control voltage	Power supply V_{DD}	2.6	2.7	5.5	V
	All control pins high, V_{ih}	1.0	2.7	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control current	All control pins high, I_{ih}		7.5		μA
	All control pins low, I_{il}		0		μA
Current consumption	I_{DD}, active mode		160	200	μA

[1] $P_{0.1dB}$ is a figure of merit. Please do not exceed Absolute Maximum ratings.
[2] From 50 % of the control signal to 10 %/90 % of the settled RF value, with $C_{VCP} = 1$ nF to GND on the V_{CP} pin.
[3] Start-up time is the time from V_{DD} ON to RF signal settled on a throw, or the transition time from low power mode to active mode.
No external DC blocking capacitors are required on the RF pins unless a DC voltage is applied on an RF pin.

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Switch Control table

Table 7: Switch Control Table

V_{DD}[1]	V_1	V_2	**Switch state**
1	0	0	All OFF[2]
1	0	1	$RFC - RF2$ ON
1	1	0	$RFC - RF1$ ON
1	1	1	All ON, $RFC - RF1$ and $RFC - RF2$ ON

[1] V_{DD} should be applied first before V_1 and V_2, otherwise may cause damage to the device.
[2] There are internal pull-downs to ground on both V_1 and V_2 control pins, the state at start-up without any control voltage applied will be All OFF.

Theory of Operation

The TS64210L is a reflective open SP2T switch: each throw is a series switch between RFC and RFx, without a shunt switch. An OFF throw is open; it is seen as its OFF capacitance $C_{OFF} = 0.28$ pF. An ON throw is seen as its ON resistance $R_{ON} = 1.1\,\Omega$. Throw $RF1$ is controlled by V_1 and throw $RF2$ by V_2, independently of each other, which gives 4 states: All OFF, $RF1$ ON, $RF2$ ON and All ON.

Application Information

The TS64210L is designed for antenna and filter tuning, dynamic matching, private mobile radio handsets and public safety handsets from 1 MHz to 3 GHz, where high RF peak voltage handling (120 V) is desired. Tuning elements connected to $RF1$ and $RF2$ can be switched to RFC one at a time, both together, or not at all.

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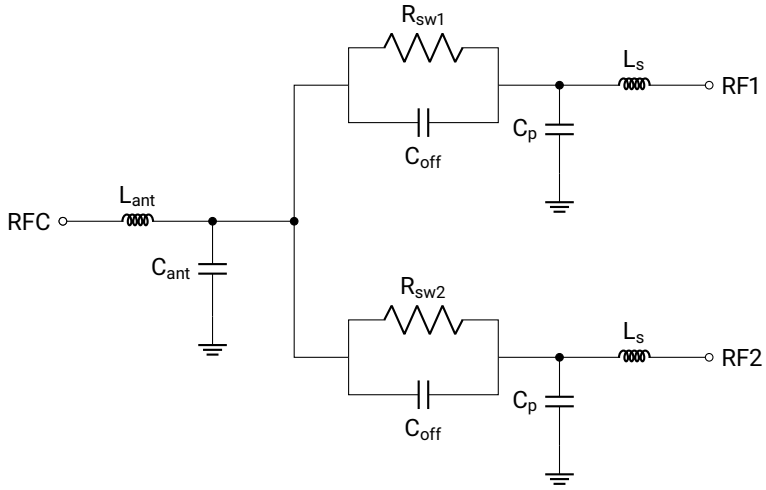
Circuit Model and Evaluation Board



Circuit model of the TS64210L

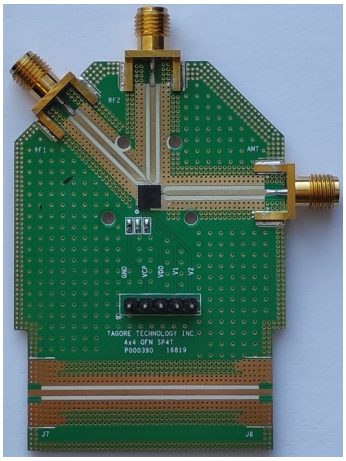


Photo of TS64210L EVB

Table 8: Recommended model values

Component	Value	Unit
C_p	0.3	pF
C_{off}	0.28	pF
R_{swx}	1.1 if ON	Ω
R_{swx}	100 k if OFF	Ω
L_s	0.4	nH
L_{ant}	0.9	nH
C_{ant}	0.5	pF

R_{ON} and R_{OFF} are measured at DC. An accurate model is available on the TagoreTech website: TS64210L Product Page.

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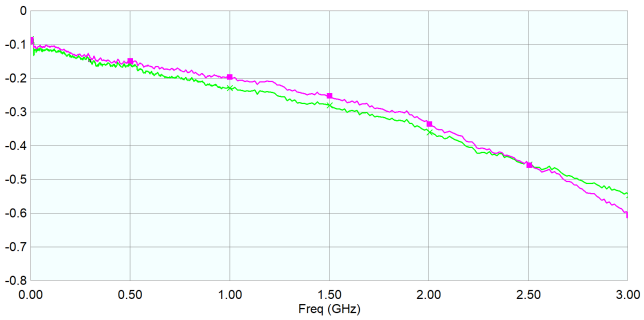
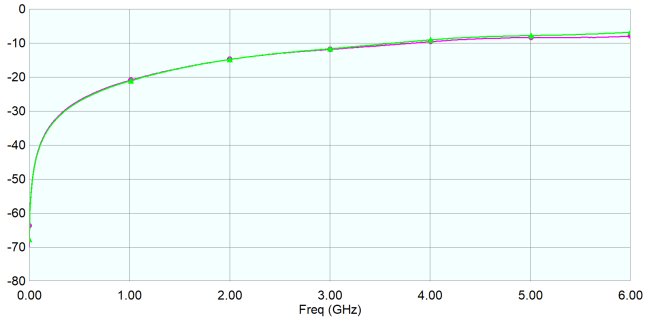
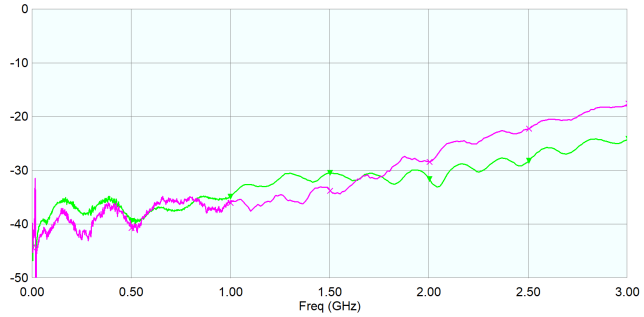
Typical characteristics



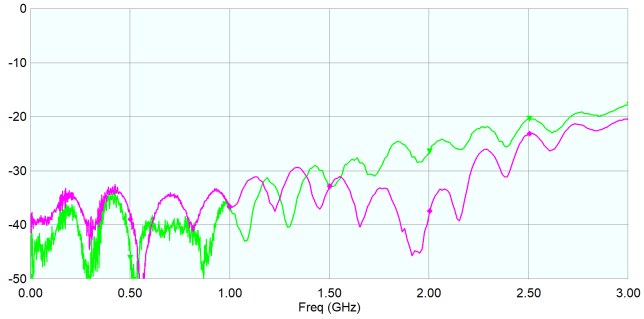
RF1, RF2 insertion loss [dB]



RF1, RF2 isolation [dB]



Return loss, RFx [dB]



Return loss, RFC [dB]

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Device Package information

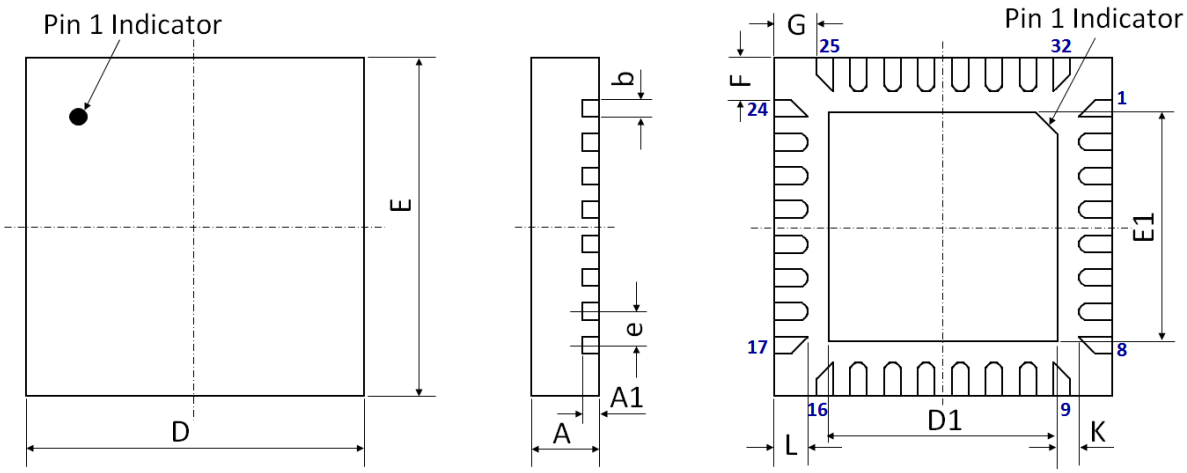

Figure 5: 32-pin QFN 4.0 x 4.0 x 0.75 mm^3 package drawing.

Please refer to application notes TN-001 PCB Design guideline and TN-002 Solder Rework at TagoreTech web page for PCB and soldering guidelines.

Table 9: Device Package Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A	0.75	±0.05	E	4.00 BSC	±0.05
A1	0.203	±0.02	E1	2.70	±0.05
b	0.20	+0.05/-0.07	F	0.50	±0.05
D	4.00 BSC	±0.05	G	0.50	±0.05
D1	2.70	±0.05	L	0.40	±0.05
e	0.40 BSC	±0.05	K	0.25	±0.05

Lead finish: pure Sn without underlayer; thickness 7.5 μm to 20 μm (typical 10 μm to 12 μm).

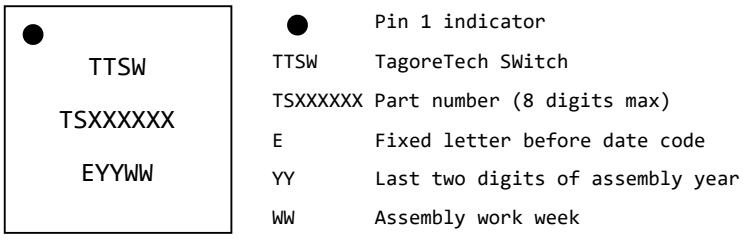

Figure 6: Part marking specification.

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PCB Land Design

Notes:

- 4-layer PCB is recommended.
- Via diameter is recommended to be 0.2 mm to prevent solder wicking inside the vias.
- Thermal vias shall only be placed on the center pad.
- The maximum via number for the center pad is 4(X)×4(Y)=16.

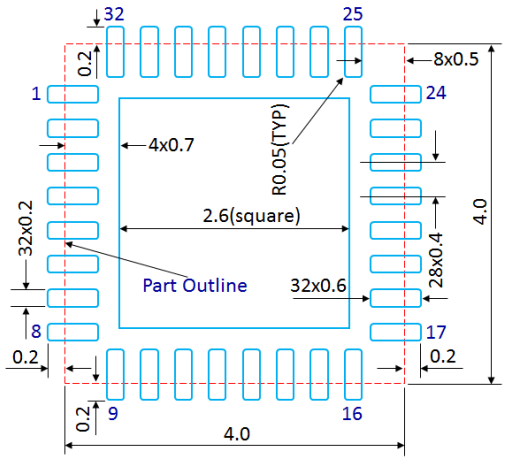

Figure 7: PCB land pattern, dimensions in [mm].



Figure 8: Solder mask pattern, non-solder mask defined (preferred, left) and solder mask defined (right), dimensions in [mm].

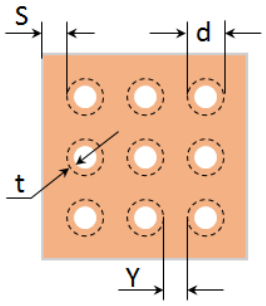

Figure 9: Thermal Via Pattern, Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm.

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PCB Stencil Design

Notes:

- Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- Stencil thickness is recommended to be 125μm.

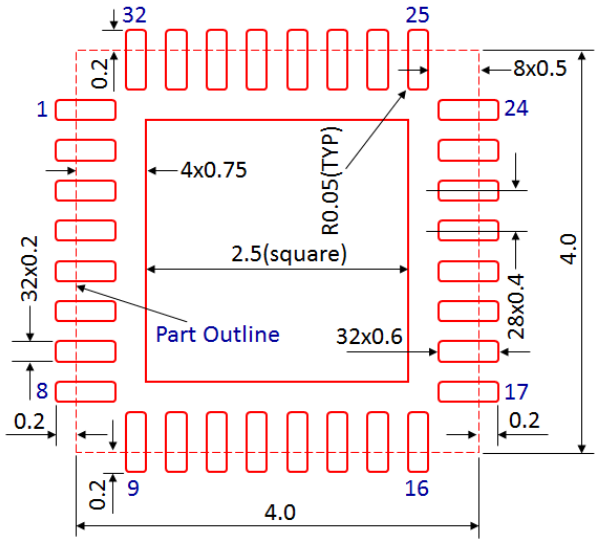

Figure 10: Stencil Openings, dimensions in [mm].

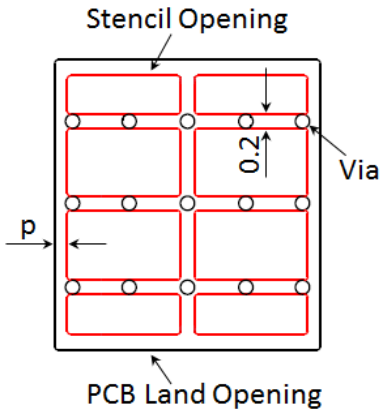

Figure 11: Stencil Openings Shall not Cover Via Areas If Possible, dimensions in [mm].

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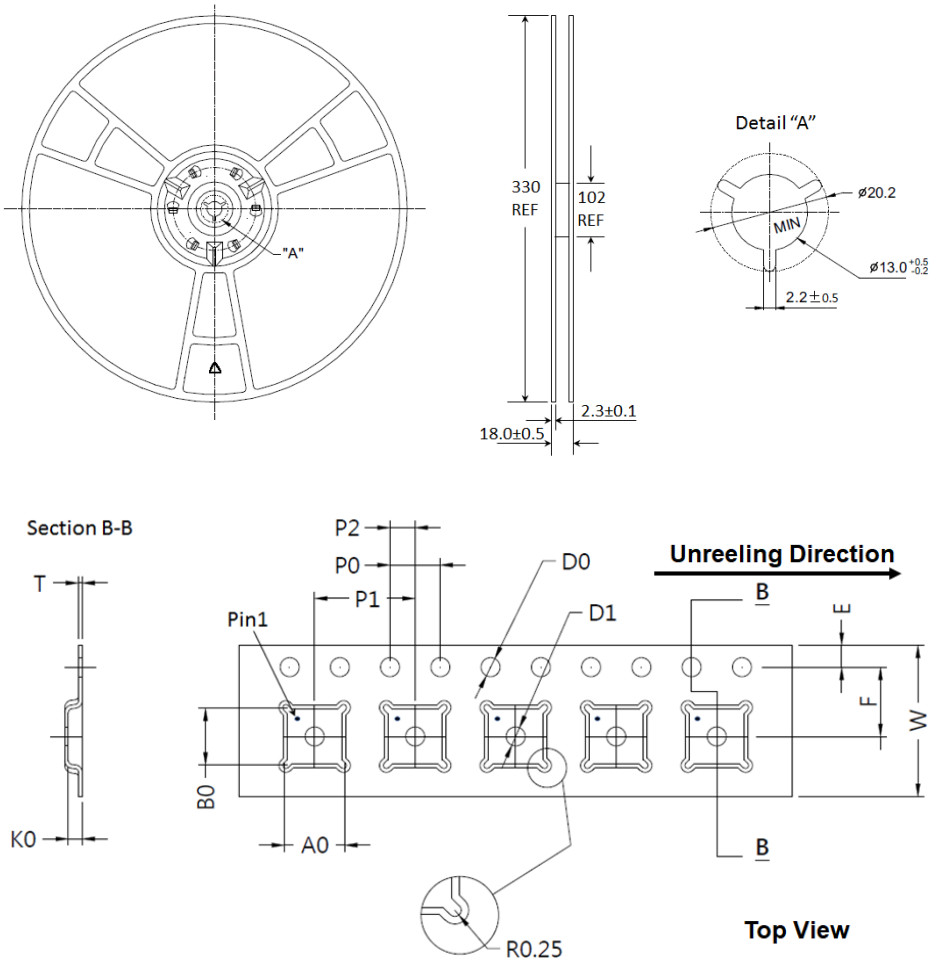
Tape and Reel Information



A0[mm]	B0[mm]	D0[mm]	D1[mm]	E[mm]	F[mm]	K0[mm]	P0[mm]	P1[mm]	P2[mm]	T[mm]	W[mm]
3.35	3.35	1.50	1.50	1.75	5.50	1.10	4.00	8.00	2.00	0.30	12.00

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Glossary

IL	Insertion loss
ISO	Isolation
RL	Return loss
VSWR	Voltage Standing Wave Ratio
RFC	Antenna port or common port, referred as RFC
RFx	RF Port number x
R_{ON}	ON resistance of a throw
C_{OFF}	OFF capacitance of a throw

Changelog

Table 10: Changelog

Date	Revision	Notes
08/23/2024	2.0	Previous datasheet revision (Word).
10/31/2026	3.00	Transferred to the TagoreTech datasheet format. Pin table corrected (RF1 pin 22, RF2 pin 19), package height 0.75 mm, return loss and harmonics shown as negative values, circuit model redrawn, links to application notes TN-001/TN-002, QR code link to the latest datasheet, glossary.

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