SPDT 10 W CW/50 W_{peak} GaN RF Switch 500 MHz to 7.0 GHz

Features

- Frequency Range 500 MHz to 7.0 GHz
- Low insertion loss: 0.5 dB @ 2.6 GHz
- High isolation: 35 dB @ 2.6 GHz
- High peak power handling capability
- 40 dBm CW hot switching capability
- No external DC blocking capacitors on RF lines
- All RF ports OFF state
- Versatile 2.6 V – 5.5 V power supply

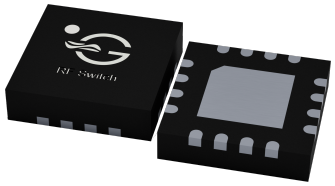

Figure 1: TS7226K in 3.0 x 3.0 mm^2 QFN 16-pin package.

Applications

- Mobile radio handsets
- Massive MIMO
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals

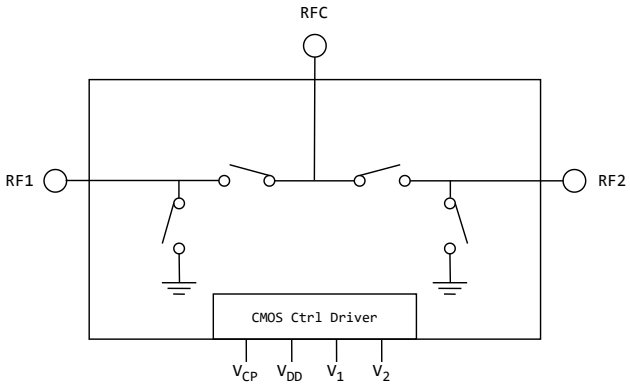

Figure 2: TS7226K functional diagram

General Description

The TS7226K is a symmetrical reflective Single Pole Double Throw (SPDT) switch designed for broadband, high peak power switching applications. Its broadband behavior from 500 MHz to 7.0 GHz makes the TS7226K an excellent switch for all applications requiring low insertion loss, high isolation, and high linearity within a small package size.

The TS7226K is housed in a compact $3.0 \times 3.0\ mm^2$ 16-lead Quad Flat No-lead (QFN) plastic package.

RoHS10/REACH/Halogen free

Contents

Features 1
Applications 1
General Description 1
Ordering information 3
Pin Assignment 4
Absolute Maximum Ratings 5
Electrical Specifications 6
Switching time definition . . . 8
Switch Control table 9
Theory of Operation 10
Feeding external V_{CP} voltage of -18 V . . . 10
Schematics and Evaluation Board 10
Typical characteristics 12
Peak power handling with modulated signals . . . 14
Peak-to-average power ratio of QAM signals . . . 14
Crest factor reduction for OFDM . . . 15
Average power capability with modulated signals . . . 15
Device Package information 17
PCB Land Design 19
PCB Stencil Design 21
Tape and Reel Information 22
Glossary 23
Changelog . . . 23
Legal Information 24
Published by . . . 24
Legal Disclaimer . . . 24
Sales Contact . . . 24
Buy TS7226K directly . . . 24
TS7226K Product information . . . 24
TagoreTech Inc. Product Brochure and datasheets . . . 24

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Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TS7226K	16 Pin 3.0x3.0x0.75 mm^3 QFN	Core part number
TS7226K-EVB	Evaluation Board	
TS7226KMTRPBF[1]	330 mm reel, 3 000 pcs	Full reel

[1] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	13” (330mm)	18mm

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Pin Assignment

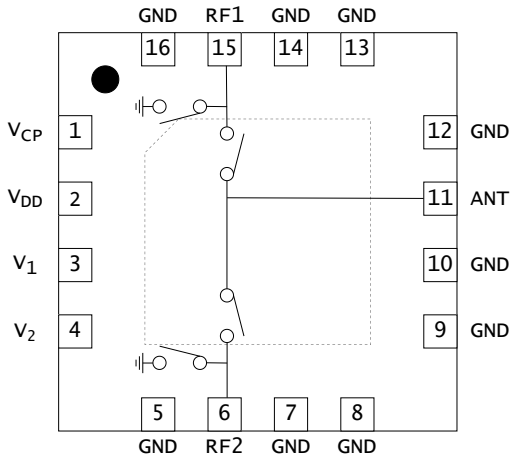

Figure 3: TS7226K pin assignment [top view]

Table 3: Pin Definition

Pin Number	Pin Name	Description
1	V_{CP}	Internal charge pump voltage output, connect a 1 nF capacitor to GND on this pin to improve switching time.
2	V_{DD}	DC Power Supply
3	V_1	Switch control input 1
4	V_2	Switch control input 2
6	RF2	RF port 2
5,7,8,9,10,12,13,14,16	GND	Connect to ground[2]
11	RFC	RF Common port (Antenna port)
15	RF1	RF port 1
17 [1]	GND	Ground thermal pad, please connect to GND

[1] The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.
[2] These pins are NC pins inside the package. To avoid floating pins around RF lines, we request these to be connected to ground.

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	V_{DD}	5.5	V
External bias voltage on V_{CP} pin	V_{CP}	-20	V
Storage Temperature Range	T_{st}	−55 – 125	°C
Operating Temperature Range	T_{op}	−40 – 85	°C
Maximum Junction Temperature	T_j	+140	°C
Maximum RF CW input power, 2600 MHz, T_J=+85°C	RFx	41.5	dBm
Maximum RF peak input power, 2600 MHz, 1% duty cycle, 10 μs pulse	RFx	48	dBm
Max RF peak voltage 500MHz	RFx / RFC	75	V
Max RF peak voltage f_{max}	RFx / RFC	75	V
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	25	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta jt}$	$\leq$39	°C/W
Soldering Temperature	T_{solder}	+260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 – $<$1000	V
Charged Device Model (CDM)	Level C3	$\geq$1000	V
Moisture Rating			
Moisture Sensitivity Level[2]	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and can cause permanent damage to the device. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.

[2] Tagore recommends to store parts in moisture barrier bag to preserve solderability.

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Electrical Specifications

Table 5: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency[1]	f	500		7000	MHz
Insertion loss	800 MHz		0.40	0.50	dB
RFC – RFx	1.95 GHz		0.45	0.55	dB
	2.6 GHz		0.50	0.65	dB
	3.8 GHz		0.60		dB
	7.0 GHz		0.90		dB
Isolation	800 MHz	45	48		dB
RFC – RFx	1.95 GHz	37	40		dB
	2.6 GHz	32	35		dB
	3.8 GHz		30		dB
	7.0 GHz		20		dB
Return Loss	800 MHz		-25		dB
RFC – RFx	1.95 GHz		-23		dB
	2.6 GHz		-18		dB
	3.8 GHz		-15		dB
	7.0 GHz		-13		dB

[1] No external DC blocking capacitors are required on RF pins unless DC voltage is applied on a RF pin.

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Table 6: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	500		7000	MHz
Harmonic Distortion					
H_2	800MHz, P_{in} =38dBm		-78		dBc
H_3	800MHz, P_{in} =38dBm		-73		dBc
IIP3	2.6GHz		72		dBm
Power and Compression point					
P_{maxCW}	Max RF CW Power		40		dBm
$P_{maxpeak}$	Max RF Peak Power, 1% duty cycle, 10μs pulse		47		dBm
$P_{0.1dB}$[2]	2.6GHz, CW	40	42.5		dBm
$P_{0.1dB}$[2]	>5GHz, CW		39		dBm
$P_{peak0.1dB}$[3]	2.6GHz, 1% duty cycle		47		dBm
Switching Time					
t_{SW}	50% CTRL 10/90% of settled RF value, C_{VCP} = 1nF		0.50		μs
Power Supply, DC					
Control voltage	Power Supply V_{DD}	2.6	3.3	5.5	V
	All control pins high[4], V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control current	All control pins high, I_{ih}			7.5	μA
	All control pins low, I_{il}		0		μA
Current consumption	I_{DD}, active mode (V_{DD} on)		160	200	μA

[2] $P_{0.1dB}$ is a figure of merit. Please do not exceed Absolute Maximum ratings.
[3] 1% duty cycle and 10 μs frame width. Peak $P_{0.1dB}$.
[4] Control voltage V_{ih} cannot be higher than V_{DD} (to avoid forward biasing of ESD diode)

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Switching time definition

Example of the definition by using 10 W/40 dBm signal. We apply 10W signal to RF port, stabilized with isolator. Isolator is needed as our switch shows to RF port approximately 4Ω impedance. Let's assume that the switch insertion loss is 0.3 dB. Therefore 90% of the RF signal is 39.55 dBm and 10% of the RF signal is 1W/30dBm. We need to take into account 0.3dB insertion loss, therefore numbers are 39.25 dBm and 29.7 dBm respectively. We change the control from low to high and our time reference point is when our control signal exceeds lower threshold value $\mathrm{V_{ihlow}}$. In certain measurements when control signal rise time is significantly shorter than RF output signal, we approximate start of the clock with 50% point of the control signal.

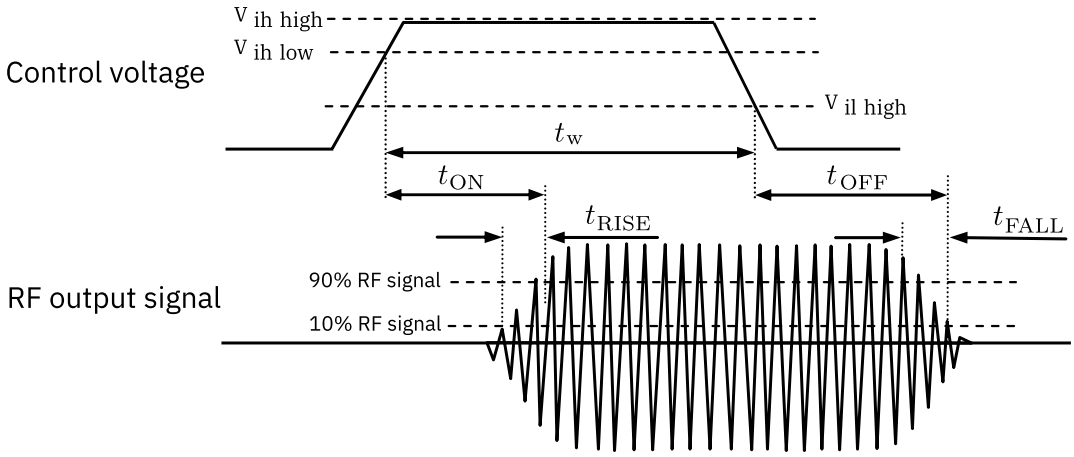

Figure 4: Switching time definition, t_{ON}, t_{OFF}, t_{RISE}, t_{FALL}. Minimum pulse width t_{w}.

Our component uses integrated charge pump. Maximum pulse repetition rate defines what is maximum frequency for switching events. Please do not exceed given maximum frequency. By feeding external -18 V to $\mathrm{V_{CP}}$, one can improve maximum pulse repetition rate f_{PRR}. Feeding external -18 V to $\mathrm{V_{CP}}$, one can drive switch at least to 20 kHz f_{PRR}. Expect current consumption of 10 mA of -18 V.

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Switch Control table

Table 7: Switch Control Table

V_{DD}[1]	V_2	V_1	**Switch state**
1	0	0	$RFC - RF1$ ON[2]
1	0	1	$RFC - RF2$ ON
1	1	0	All OFF[3]

[1] V_{DD} should be applied first before V_1 and V_2, otherwise may cause damage to the device.
[2] There are internal pull-downs to ground on both V_1 and V_2 control pins, the state at start-up without any control voltage applied will be $RFC - RF1$ ON.
[3] If All OFF state is not used, the switch can be operated with single control pin V_1

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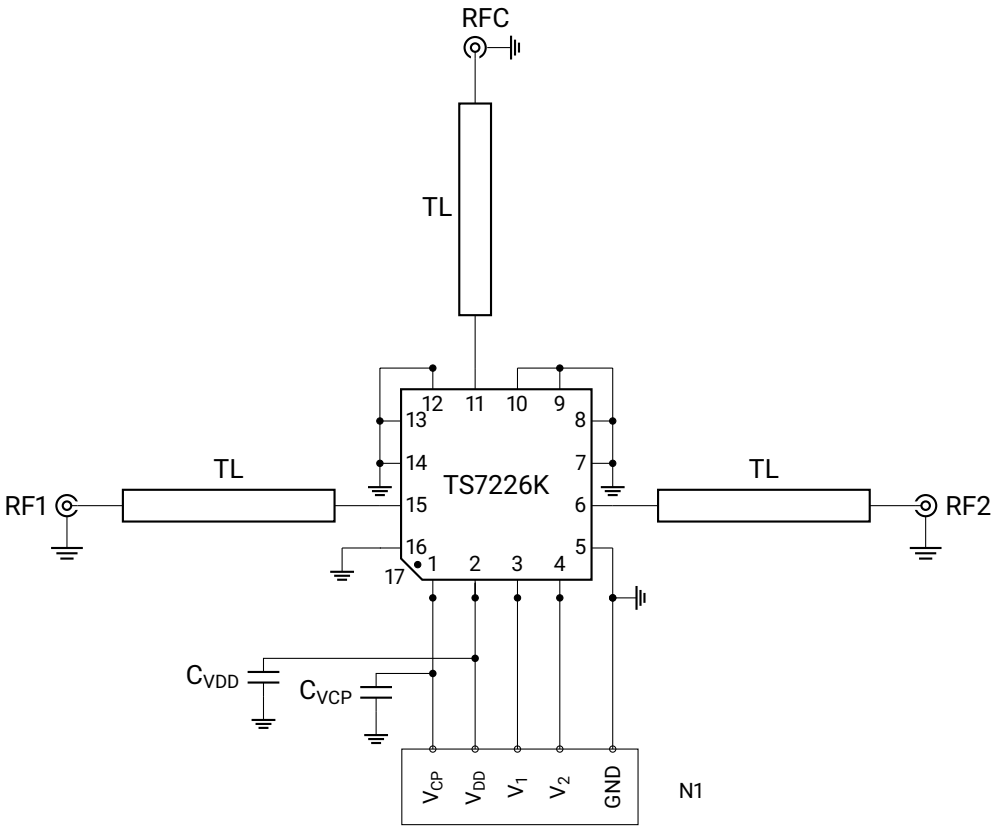
Theory of Operation

Feeding external V_{CP} voltage of -18 V

TS7226K supports external voltage supply to V_{CP} to increase pulse repetition rate f_{PRR}. With external voltage supply, f_{PRR} can be increased at least to support pulse repetition rate more than 20 kHz, in some cases even up to 100 kHz. In order to use external voltage, it is mandatory to supply first V_{DD}, have a delay of 50 μs and then apply -18 V to V_{CP}. Shutdown should be in opposite order.

Schematics and Evaluation Board

Only two external components are recommended, 1 nF for V_{CP} and 10 nF for V_{DD} lines. Pin 17 in the schematic refers to the center (thermal) pad of the device.



Schematics of TS7226K EVB

Table 8: Components used for TS7226K EVB

Reference	Part number / Value	Description	Notes
C_{VDD}	10 nF	Capacitor	GRM155R71H103KA88
C_{VCP}	1 nF	Capacitor	GRM155R71H102KA01D

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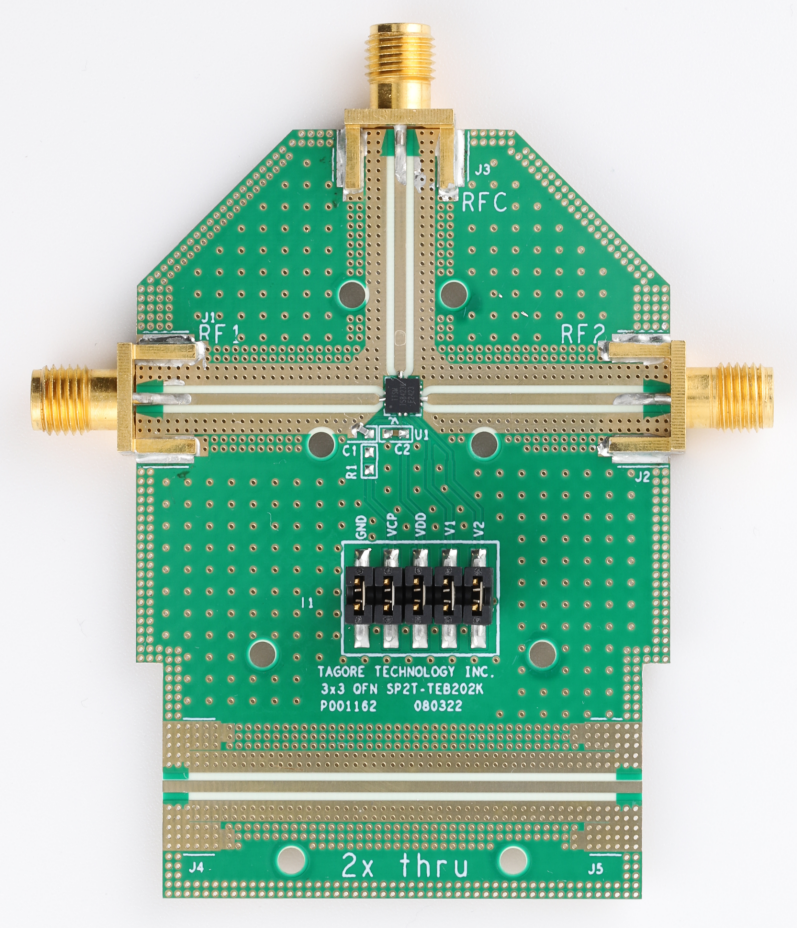

Photo of TS7226K EVB

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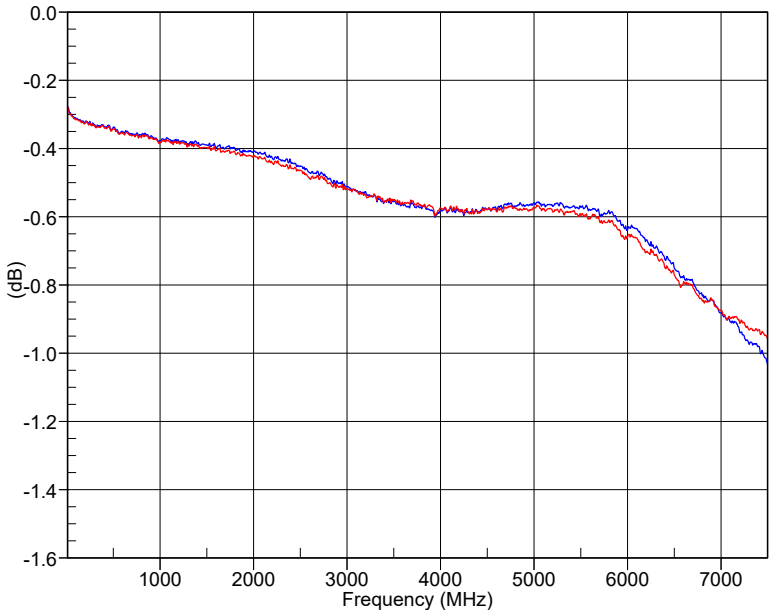
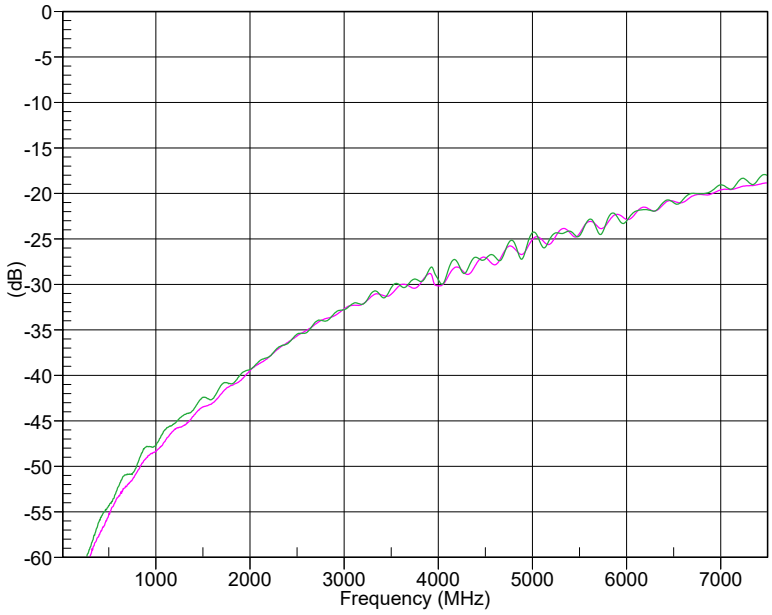
Typical characteristics

These measurements have been taken from TS7226K EVB.



Insertion loss, RFC – RFx.



Isolation, RFC – RFx.

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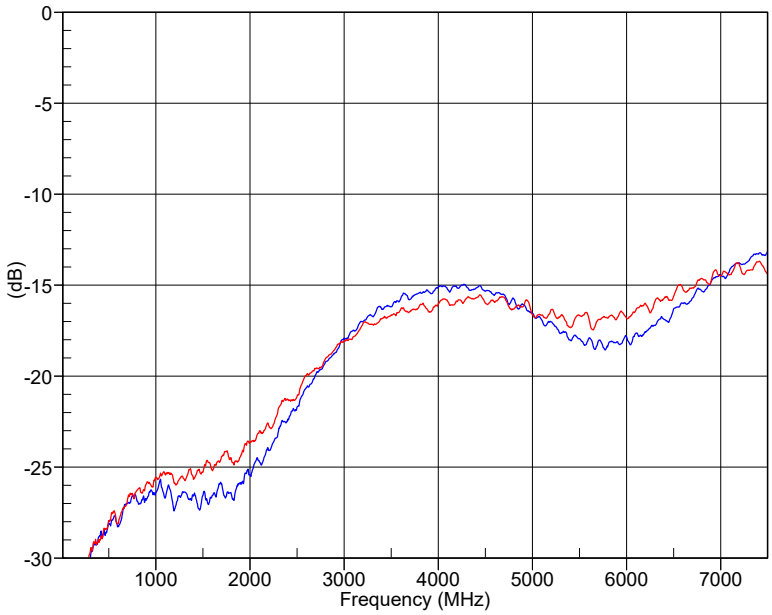
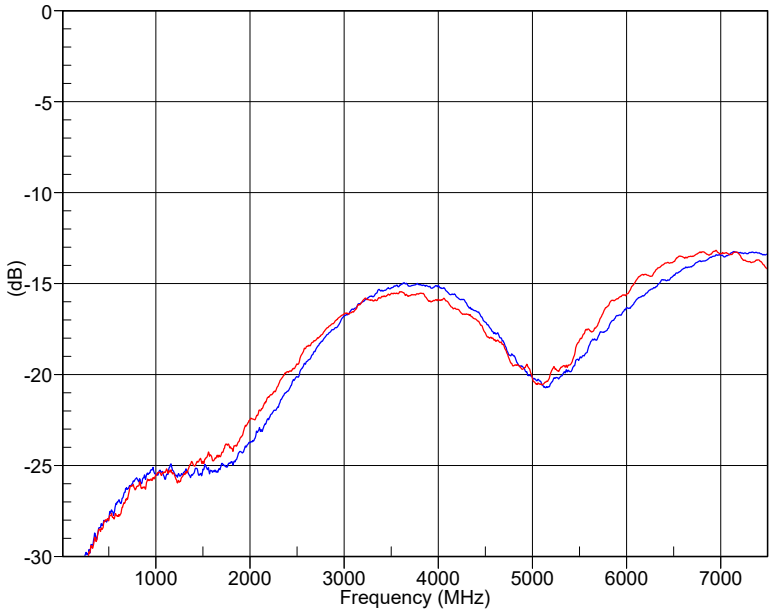


RF1, RF2 Return loss.



RFC (Antenna port) Return loss.

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Peak power handling with modulated signals

The TS7226K is rated for 40 dBm (10 W) average power (CW, 100% duty cycle) and 47 dBm (50 W) peak power, where the peak power rating is characterized with 10 μs pulses at 1% duty cycle. The two ratings describe two different physical limits of the switch. The average power rating is a thermal limit: the power dissipated in the switch, and therefore the junction temperature, is set by the average RF power. The peak power rating is a voltage limit: the instantaneous RF voltage across the OFF-state transistors must remain below their breakdown voltage. At 47 dBm in a 50 Ω system, the RF peak voltage is 71 V.

Gallium Nitride is particularly well suited for this task. The high breakdown field of GaN allows a switch to sustain high RF peak voltages, so that the peak power capability of the TS7226K exceeds its average power rating by a factor of five (7 dB). A switch whose peak capability is equal to its average rating must be derated by the full peak-to-average ratio of the signal, whereas the TS7226K can handle the envelope peaks of single-carrier and OFDM modulated signals with little or no back-off.

Peak-to-average power ratio of QAM signals

Quadrature amplitude modulation (QAM), such as 16-QAM, 64-QAM or 256-QAM, does not have a constant envelope. The instantaneous envelope power fluctuates around the average power, and its peaks can be several dB above the average. The peaks are statistical in nature: the higher the level, the smaller the fraction of time for which the envelope exceeds it. This behavior is described by the complementary cumulative distribution function (CCDF) of the signal. The peak-to-average power ratio (PAPR) at a probability p is the level, relative to the average power, which the envelope exceeds for a fraction p of the time.

For single-carrier QAM, the PAPR is set by the constellation and by the pulse-shaping filter: a smaller root-raised-cosine (RRC) roll-off factor α gives a narrower spectrum but higher envelope peaks. For OFDM, the sum of many independently modulated subcarriers produces a nearly Gaussian signal, and the PAPR is practically independent of the QAM order of the subcarriers. OFDM therefore has a clearly higher PAPR than single-carrier QAM.

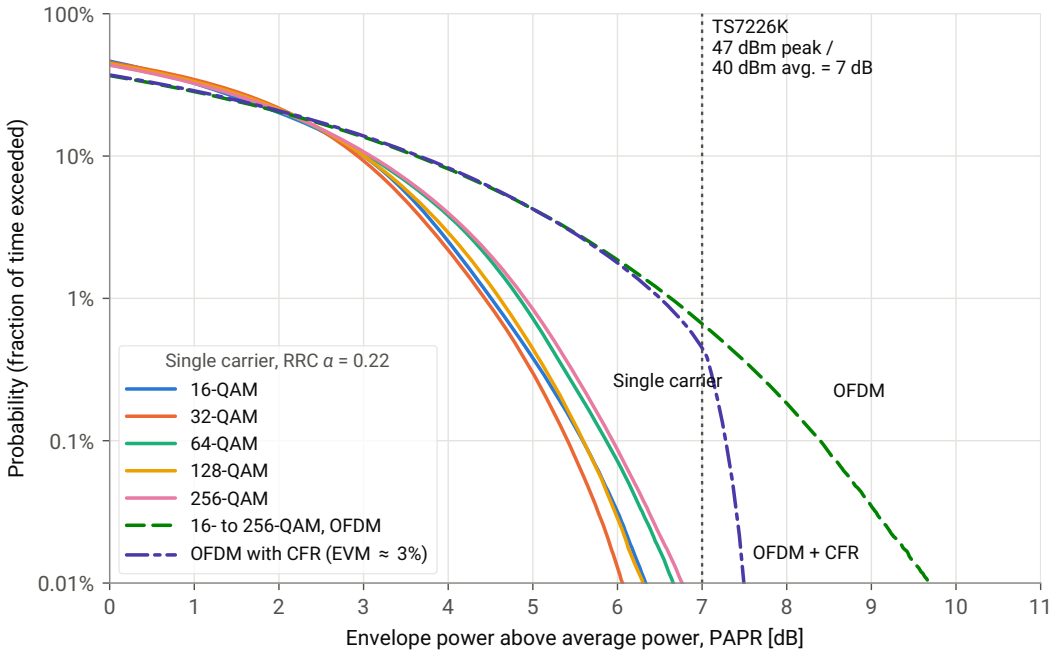

Figure 5: CCDF of the envelope power of QAM signals: fraction of time the envelope power exceeds the average power by the given PAPR. OFDM with CFR: iterative clipping and filtering, EVM ≈ 3%. The dotted line marks the 47 dBm / 40 dBm (7 dB) peak-to-average capability of the TS7226K.

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Crest factor reduction for OFDM

Because the highest envelope peaks of an OFDM signal are rare, practical OFDM transmitters apply crest factor reduction (CFR) in the digital baseband before the power amplifier. A common method is iterative clipping and filtering: the envelope is limited to a threshold above its average, and the spectral regrowth caused by the clipping is filtered away, so that the transmitted spectrum and adjacent-channel leakage are preserved. The price is in-band distortion, expressed as an increase in error vector magnitude (EVM). The amount of CFR that can be applied is therefore set by the EVM budget of the modulation: 16-QAM tolerates considerably more distortion than 256-QAM. CFR removes only the rare, highest peaks; the PAPR at 1% to 10% probability is practically unchanged, while the PAPR at 0.1% is reduced by 0.4 dB to 1.9 dB for EVM contributions of 1.5% to 5%. Table 9 includes typical values for OFDM with CFR.

Average power capability with modulated signals

Typical PAPR values are listed in Table 9. Figure 5 shows the complete CCDF curves together with the 7 dB peak-to-average capability of the TS7226K. At the full 40 dBm average rating, the envelope of a single-carrier 16- to 256-QAM signal practically never exceeds the 47 dBm peak level (less than 0.01% of the time). An OFDM signal exceeds the same level about 0.7% of the time without CFR and about 0.4% with CFR, which is within the 1% duty cycle of the peak power rating. If the envelope peaks are required to stay within 47 dBm also at the 0.1% probability level, the average power of OFDM signals is limited to the values given in the last column of the table. The envelope peaks of modulated signals last only a fraction of a symbol period, which is much shorter than the 10 μs pulses used for the peak power characterization.

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Table 9: Peak-to-average power ratio (PAPR) of QAM signals, exceeded for the given fraction of time.

Modulation	PAPR [dB] at probability[2]			TS7226K max. avg. power [W][1]
	10%	1%	0.1%	
Single carrier, RRC pulse shaping, $\alpha = 0.22$				
16-QAM	3.0	4.5	5.6	10.0
32-QAM	2.9	4.4	5.4	10.0
64-QAM	3.1	4.8	5.8	10.0
128-QAM	3.0	4.6	5.6	10.0
256-QAM	3.1	4.9	5.9	10.0
Single carrier, RRC pulse shaping, $\alpha = 0.35$				
16-QAM	3.0	4.4	5.1	10.0
32-QAM	3.0	4.2	4.8	10.0
64-QAM	3.0	4.8	5.6	10.0
128-QAM	3.0	4.5	5.2	10.0
256-QAM	3.1	4.8	5.7	10.0
OFDM, 1024 subcarriers, no crest factor reduction				
16-QAM	3.6	6.6	8.4	7.3
32-QAM	3.6	6.6	8.4	7.3
64-QAM	3.6	6.6	8.4	7.3
128-QAM	3.6	6.6	8.4	7.3
256-QAM	3.6	6.6	8.4	7.3
OFDM, 1024 subcarriers, with crest factor reduction (clipping and filtering)[3]				
CFR for EVM ≈ 1.5%, e.g. 256-QAM	3.6	6.6	8.0	8.0
CFR for EVM ≈ 3%, e.g. 64/128-QAM	3.7	6.5	7.3	9.4
CFR for EVM ≈ 5%, e.g. 16/32-QAM	3.7	6.2	6.5	10.0

[1] Average power at which the envelope peaks at the 0.1% probability level remain within the 47 dBm (50 W) peak power rating, $P_{\text{avg}} = 50\,\text{W}/10^{\text{PAPR}_{0.1\%}/10}$, limited to the 40 dBm (10 W) average power rating. Indicative values; in a mismatched load (VSWR > 1) the RF peak voltage increases and further back-off may be required.

[2] PAPR values are calculated from the envelope power of ideal, unclipped signals. Measured values depend on the transmitter, its filtering, and any crest factor reduction applied.

[3] Iterative clipping and filtering, 4 iterations, clipping level 8.0 dB, 7.0 dB and 6.0 dB above the average power; EVM is the in-band distortion added by the CFR only. The PAPR after CFR is practically independent of the QAM order; the QAM orders given are examples of modulations whose EVM budget typically allows the stated CFR. Actual CFR performance depends on the implementation.

The QAM and OFDM information in this section is provided for information only. It is based on calculated signal statistics, has not been fully characterized on the TS7226K, and is not binding on TagoreTech; the ratings given in the Absolute Maximum Ratings and Electrical Specifications sections apply.

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Device Package information

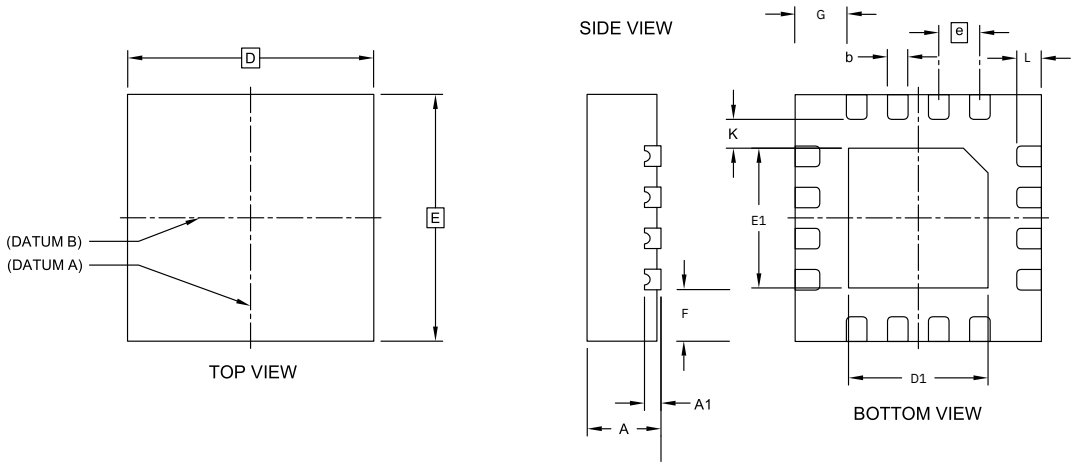

Figure 6: 16-pin QFN 3.0 x 3.0 x 0.75 mm^3 package drawing.

Please refer to application notes TN-001 PCB Design guideline and TN-002 Solder Rework at TagoreTech web page for PCB and soldering guidelines.

Table 10: Device Package Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A	0.75	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Lead finish: Pure Sn without underlayer; thickness 7.5 μm – 20 μm (typical 10 – 12 μm).

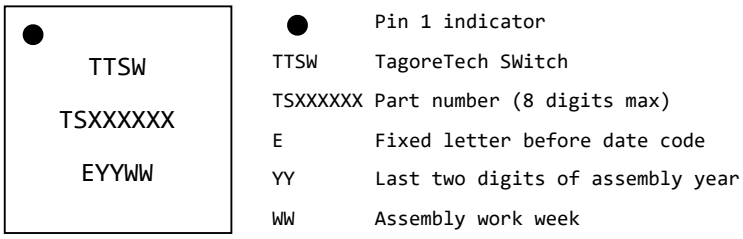

Figure 7: Part marking specification.

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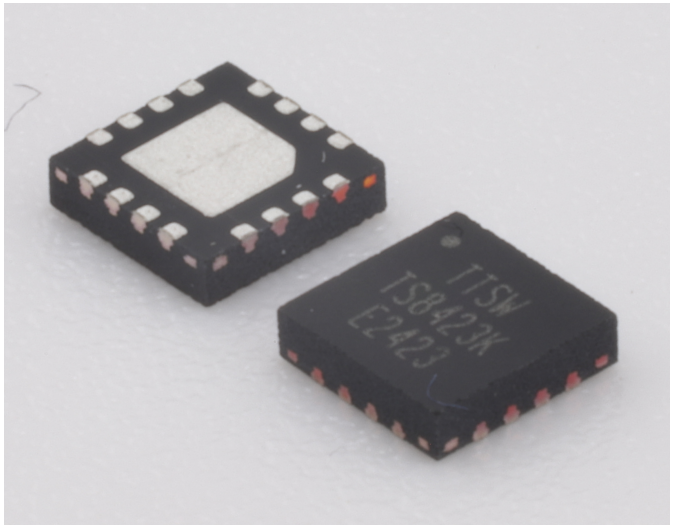

Figure 8: TS7226K photo, top and bottom side.

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PCB Land Design

Notes:

- 4-layer PCB is recommended.
- Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
- Thermal vias shall only be placed on the center pad.
- The maximum via number for the center pad is 3(X)×3(Y)=9.

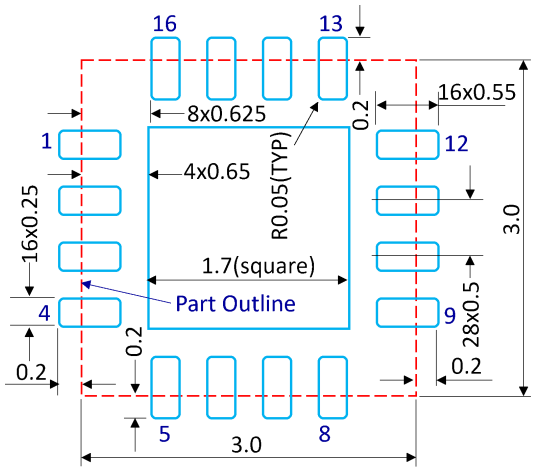

Figure 9: PCB land pattern, dimensions in [mm].

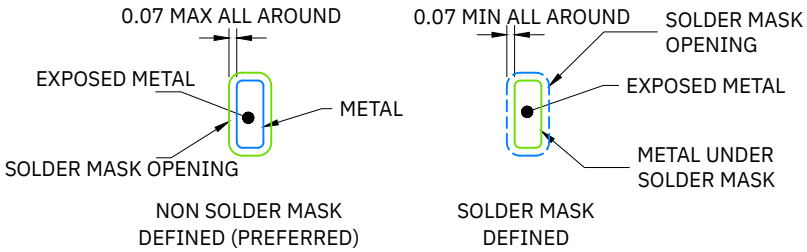

Figure 10: Solder mask opening, dimensions in [mm].

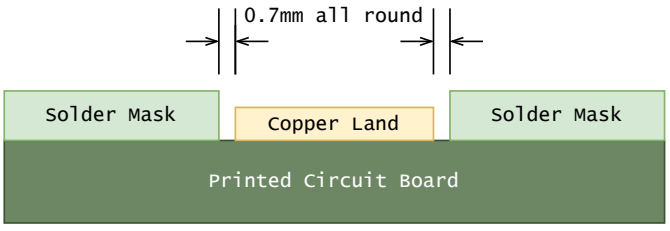

Figure 11: Preferred solder mask opening, side view, dimensions in [mm].

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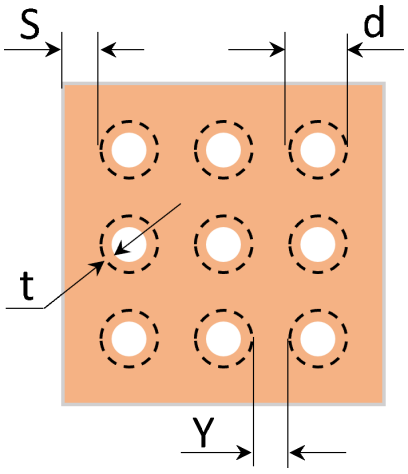

Figure 12: Thermal Via Pattern, Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm.

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PCB Stencil Design

Notes:

- Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- Stencil thickness is recommended to be 125μm.

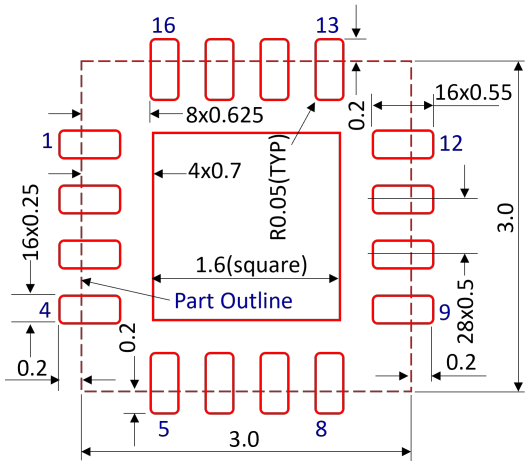

Figure 13: Stencil Openings, dimensions in [mm].

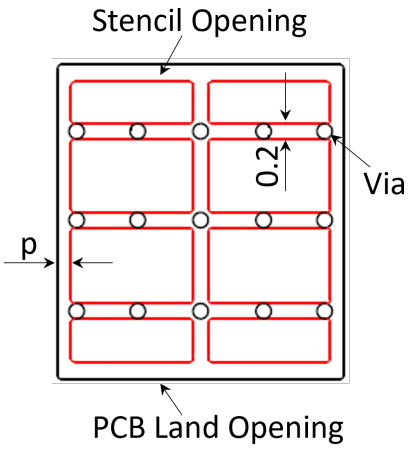

Figure 14: Stencil Openings Shall not Cover Via Areas If Possible, dimensions in [mm].

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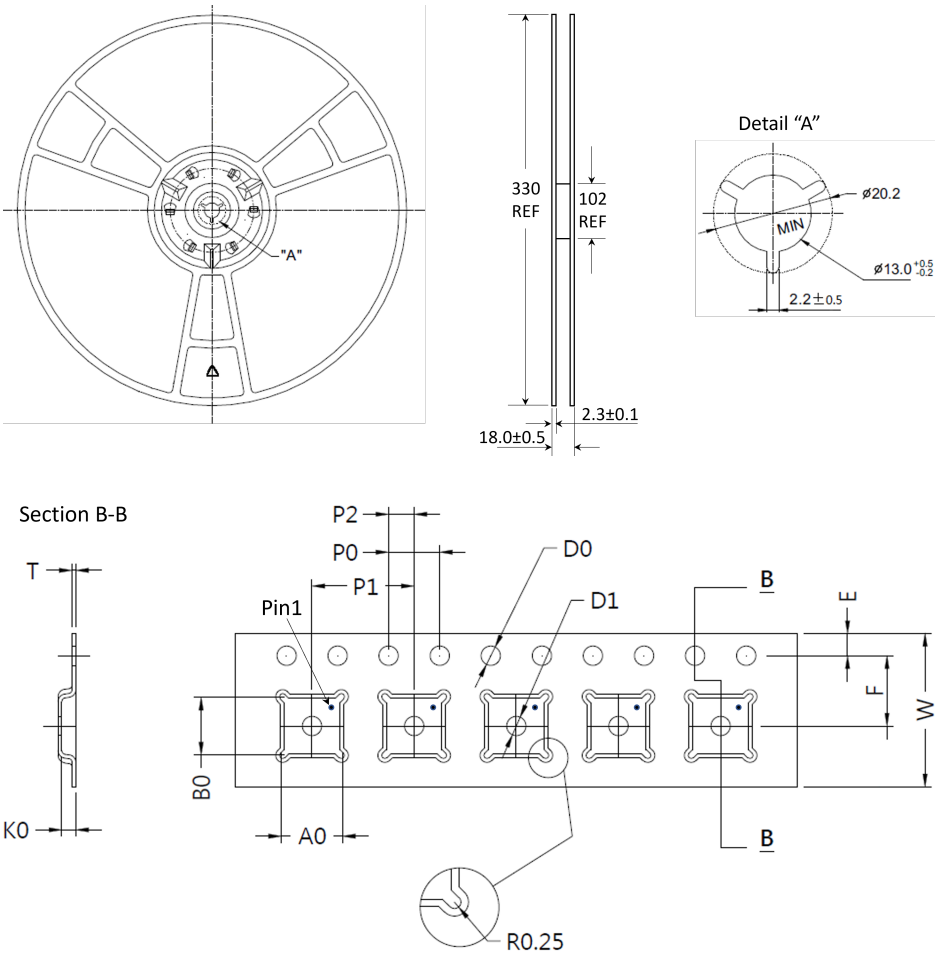
Tape and Reel Information



A0[mm]	B0[mm]	D0[mm]	D1[mm]	E[mm]	F[mm]	K0[mm]	P0[mm]	P1[mm]	P2[mm]	T[mm]	W[mm]
3.35	3.35	1.50	1.50	1.75	5.50	1.10	4.00	8.00	2.00	0.30	12.00

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Glossary

IL	Insertion loss
ISO	Isolation
RL	Return loss
VSWR	Voltage Standing Wave Ratio
RFC	Antenna port or common port, referred as RFC
RFx	RF Port number x
CCDF	Complementary cumulative distribution function
CFR	Crest factor reduction
EVM	Error vector magnitude
OFDM	Orthogonal frequency-division multiplexing
PAPR	Peak-to-average power ratio
QAM	Quadrature amplitude modulation
RRC	Root-raised-cosine (pulse-shaping filter)

Changelog

Table 11: Changelog

Date	Revision	Notes
09/04/2024	2.0	TS7226K datasheet, previous format.
09/20/2026	3.00	Datasheet converted to common TagoreTech datasheet template, package thickness corrected to 0.75mm, $\mathrm{V_{CP}}$ absolute maximum rating added.
10/26/2026	3.01	Peak power handling with modulated signals added: PAPR of QAM and OFDM signals, crest factor reduction, CCDF plot. P_{maxCW} 40 dBm and P_{maxpeak} 47 dBm added to the electrical specification; RF peak input power 48 dBm and RF peak voltage 75 V added to the absolute maximum ratings. QR code link to the latest datasheet, links to application notes TN-001/TN-002, distributor table reformatted, glossary extended. $\mathrm{V_{DD}}$ to $\mathrm{V_{CP}}$ delay 50 μs, EVB capacitor part numbers added.

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