SP4T 10 W/63 W_{peak} Power Switch 0.4 GHz to 3.8 GHz

Features

- Frequency Range 400 MHz to 3.8 GHz
- Low insertion loss:
  0.40 dB @ 800 MHz
  0.60 dB @ 2.6 GHz
- High isolation: 45 dB @ 800 MHz
- 10 W CW Power, 63 W_{peak} Peak Power
- 40 dBm CW hot switching capable
- 4 independent control inputs, 16 switch states
- Series and shunt switch in each throw
- No external DC blocking capacitors on RF lines
- Versatile 2.6 V – 5.5 V power supply
- No need to supply negative voltages

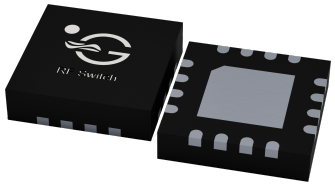

Figure 1: TS72461K in 3.0 x 3.0 mm^2 QFN 16-pin package.

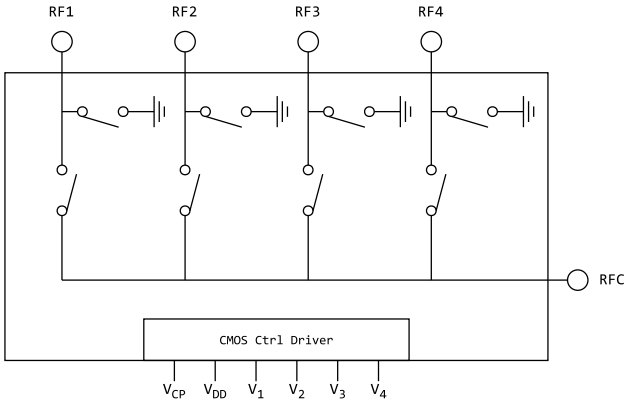

Figure 2: TS72461K functional diagram

Applications

- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals

General Description

The TS72461K is a symmetrical reflective Single Pole Four Throw (SP4T) GaN switch designed for broadband and high power switching applications. The TS72461K covers 400 MHz to 3.8 GHz and provides low insertion loss, high isolation and high linearity within a small package size. Each throw has a series and a shunt switch. The four control inputs V_1 to V_4 control the four throws independently, which gives up to 16 switch states.

The TS72461K is housed in a compact 3.0×3.0 mm^2 16-lead Quad Flat No-lead (QFN) plastic package.

RoHS

RoHS10/REACH/Halogen free

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Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TS72461K	16 Pin 3.0x3.0x0.75 mm^3 QFN	Core part number
TS72461K-EVB	Evaluation Board	
TS72461KMTRPBF[1]	330 mm reel, 3 000 pcs	Full reel

[1] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	13” (330mm)	18mm

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Pin Assignment

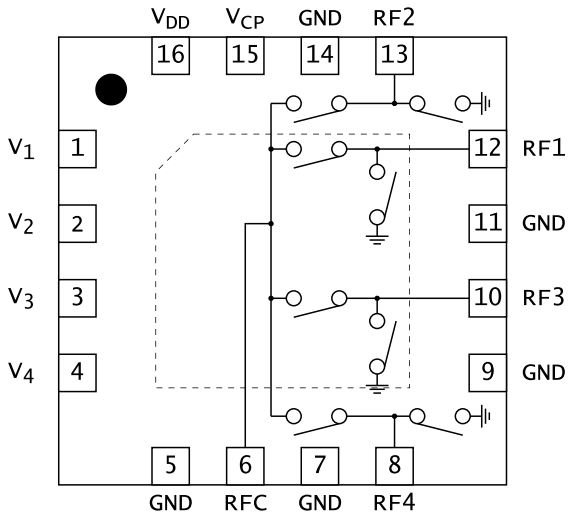

Figure 3: TS72461K pin assignment [top view]

Table 3: Pin Definition

Pin Number	Pin Name	Description
1	V_1	Switch control input 1 (RFC – RF1)
2	V_2	Switch control input 2 (RFC – RF2)
3	V_3	Switch control input 3 (RFC – RF3)
4	V_4	Switch control input 4 (RFC – RF4)
6	RFC	RF Common port (ANT)
8	RF4	RF port 4
10	RF3	RF port 3
12	RF1	RF port 1
13	RF2	RF port 2
15	V_{CP}	Internal charge pump voltage output. Connect a 1 nF capacitor to GND on this pin to improve switching time.
16	V_{DD}	DC Power Supply
5, 7, 9, 11, 14	GND	Connect to ground[2]
17 [1]	GND	Ground thermal pad, please connect to GND

[1] The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.
[2] These pins are NC pins inside the package. To avoid floating pins around RF lines, we request these to be connected to ground.

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	V_{DD}	5.5	V
External bias voltage on V_{CP} pin	V_{CP}	-20	V
Storage Temperature Range	T_{st}	−55 – 125	°C
Operating Temperature Range	T_{op}	−40 – 85	°C
Maximum Junction Temperature	T_j	+150	°C
Maximum RF CW input power, $T_{case} = +85$°C	RFx / RFC	41	dBm
Maximum RF peak input power, 1% duty cycle, $T_{case} = +85$°C	RFx / RFC	49	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	$\leq$20	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta jt}$	$\leq$37	°C/W
Soldering Temperature	T_{solder}	+260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 – $<$1000	V
Charged Device Model (CDM)	Level C3	$\geq$1000	V
Moisture Rating			
Moisture Sensitivity Level[2]	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and can cause permanent damage to the device. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.

[2] Tagore recommends to store parts in moisture barrier bag to preserve solderability.

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Electrical Specifications

Table 5: Electrical Specifications $T_A = +25°C; V_{DD} = +2.7V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	400		3800	MHz
Insertion loss	800 MHz		0.40		dB
unmatched, $RFC - RFx$	1.95 GHz		0.50		dB
	2.6 GHz		0.60	0.80	dB
Insertion loss[1], matched	3.8 GHz		0.90		dB
Isolation	800 MHz		45		dB
unmatched, $RFC - RFx$	1.95 GHz		33		dB
	2.6 GHz	22	28		dB
Isolation[1], matched	3.8 GHz		23		dB
Return loss	800 MHz		-28		dB
unmatched, $RFC - RFx$	1.95 GHz		-25		dB
	2.6 GHz		-18		dB
Return loss[1], matched	3.8 GHz		-15		dB

[1] Matched for 3.3 to 3.8 GHz, see Schematics and Evaluation Board. Matched values are not guaranteed as they include performance of matching components. These components are beyond control of TagoreTech and therefore given values are indications, not guaranteed values.

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Table 6: Electrical Specifications $T_A = +25°C; V_{DD} = +2.7V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Harmonic Distortion					
H_2	800 MHz, P_{in} =35 dBm		-42		dBm
H_3	800 MHz, P_{in} =35 dBm		-45		dBm
IIP3	800 MHz		70		dBm
Power and Compression point					
$P_{0.1dB}$[1]	CW, 800 to 3800 MHz, -40 to $+85°C$	40			dBm
$P_{peak\,0.1dB}$[1]	1 % duty cycle, 800 to 3800 MHz, -40 to $+85°C$		48		dBm
$P_{max\,hot}$[2]	Max RF CW power, hot switching		40		dBm
Switching Time					
t_{SW}[3]	Switching time, $C_{VCP} = 1$ nF		1.2		μs
Power Supply, DC					
Control voltage	Power supply V_{DD}	2.6	3.3	5.5	V
	All control pins high, V_{ih}	1.1	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control current	All control pins high, I_{ih}			7.5	μA
	All control pins low, I_{il}		0		μA
Current consumption	I_{DD}, active mode		160	200	μA

[1] $P_{0.1dB}$ is a figure of merit. Please do not exceed Absolute Maximum ratings.
[2] Dependent on thermal design and surrounding circuits.
[3] From 50 % of the control signal to 10 %/90 % of the settled RF value, with $C_{VCP} = 1$ nF to GND on the V_{CP} pin. No external DC blocking capacitors are required on the RF pins unless a DC voltage is applied on an RF pin.

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Switching time definition

Example of the definition by using 10 W/40 dBm signal. We apply 10W signal to RF port, stabilized with isolator. Isolator is needed as our switch shows to RF port approximately 4Ω impedance. Let's assume that the switch insertion loss is 0.3 dB. Therefore 90% of the RF signal is 39.55 dBm and 10% of the RF signal is 1W/30dBm. We need to take into account 0.3dB insertion loss, therefore numbers are 39.25 dBm and 29.7 dBm respectively. We change the control from low to high and our time reference point is when our control signal exceeds lower threshold value V_{ihlow}. In certain measurements when control signal rise time is significantly shorter than RF output signal, we approximate start of the clock with the 50% point of the control signal.

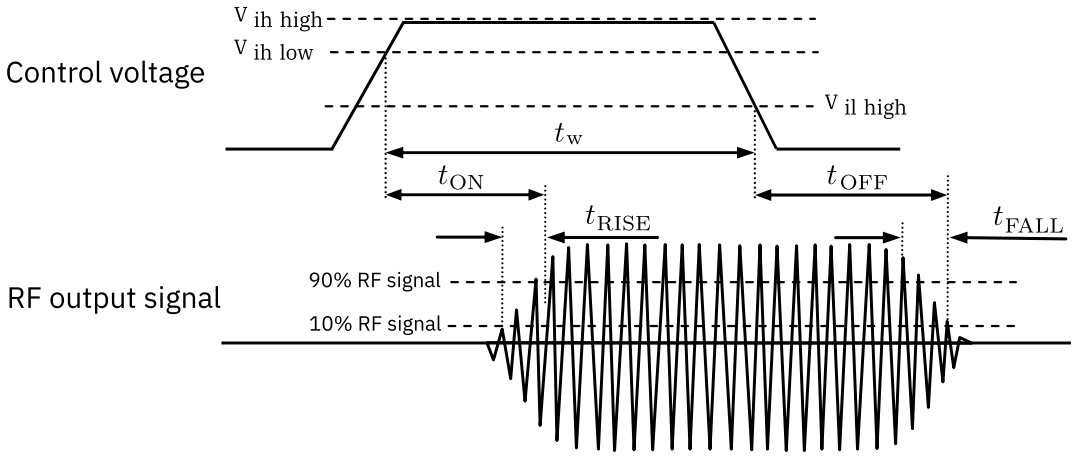

Figure 4: Switching time definition, t_{ON}, t_{OFF}, t_{RISE}, t_{FALL}. Minimum pulse width t_w.

Our component uses integrated charge pump. The switching time of the TS72461K is given with $C_{VCP} = 1$ nF on the V_{CP} pin.

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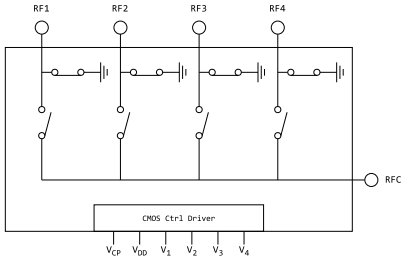
Switch Control table

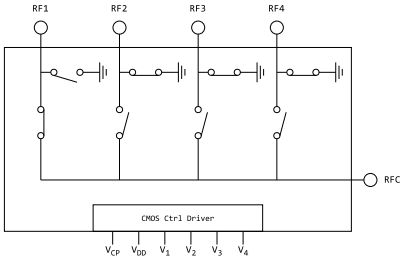
Table 7: Switch Control Table

V_{DD}[1]	V_4	V_3	V_2	V_1[2]	**Switch state**
1	x	x	x	1	RFC – RF1 ON
1	x	x	1	x	RFC – RF2 ON
1	x	1	x	x	RFC – RF3 ON
1	1	x	x	x	RFC – RF4 ON
1	0	0	0	0	RFC – RFx ALL RF switch throws OFF[3], RFC open, RF1 – RF4 shorted to GND
1	1	1	1	1	RFC – RFx ALL switch throws are ON, ie. conducting
0	0	0	0	0	V_{DD} OFF, RFC – RFx ALL switch throws are ON, ie. conducting; all series and shunt FETs are on, short shown to RFC and RF ports

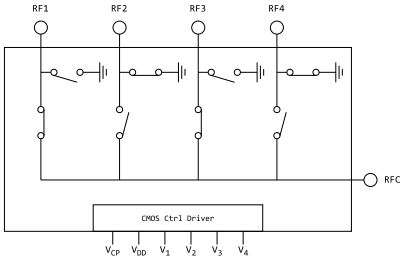
[1] V_{DD} should be applied first before V_1, V_2, V_3, and V_4, otherwise may cause damage to the device.
[2] x means any state, so all switch throws can be controlled independently. $V_x = 1$: series switch of RFx ON, shunt switch of RFx OFF. $V_x = 0$: series switch of RFx OFF, shunt switch of RFx ON.
[3] There are internal pull-downs to ground on the control pins V_1 to V_4, the state at start-up without any control voltage applied will be ALL OFF.



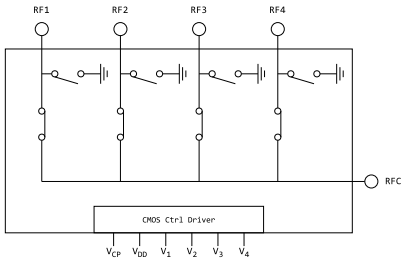
All OFF



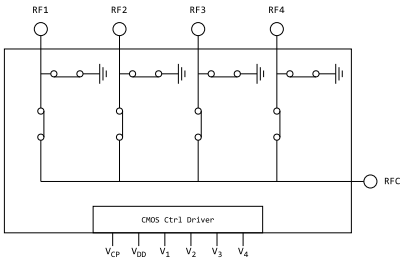
RFC-RF1 ON ($V_1 = 1$)



RFC-RF1 and RFC-RF3 ON ($V_1 = V_3 = 1$)



All ON



V_{DD} off state

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Theory of Operation

Independent control of the throws

Each throw of the TS72461K has a series switch between RFC and RFx and a shunt switch between RFx and ground. Control input V_x controls throw RFx: with V_x high, the series switch is ON and the shunt switch is OFF, and RFx is connected to RFC. With V_x low, the series switch is OFF and the shunt switch is ON, and RFx is shorted to ground. The four throws are controlled independently, which gives 16 switch states: one throw ON, several throws ON at the same time (connected in parallel to RFC), all throws ON, or all throws OFF.

Isolation modes

TS72461K has two isolation modes, the All OFF state and the V_{DD} off state.

Device powered, All OFF state

With V_1 to V_4 low, all series switches are OFF, ie. open, and all shunt switches are ON, ie. closed. RFC port is open, whereas the RFx ports are showing effectively short. This is also the start-up state, as there are internal pull-downs on the control pins.

Device powered off

When V_{DD} is 0V, all switch RF transistors are on, ie. every FET is on. This means that series FETs and shunt FETs are conducting. Every RF port is essentially connected to ground, including RFC port. This is practical when device is directly connected to the antenna, there is certain protection against induced electrical fields. This can partially protect radio equipment against electrical fields, when device is not in usage.

Applications

TS72461K is offering 10 W CW and 63 W_{peak} capability from 400 MHz to 3.8 GHz for cellular infrastructure, small cells, LTE relays and microcells and satellite terminals. The independent control of the four throws allows, for example, band and antenna selection with more than one path connected at the same time. TS72461K works without external matching components up to 2.6 GHz; the datasheet provides an example matching for 3.3 to 3.8 GHz and its performance.

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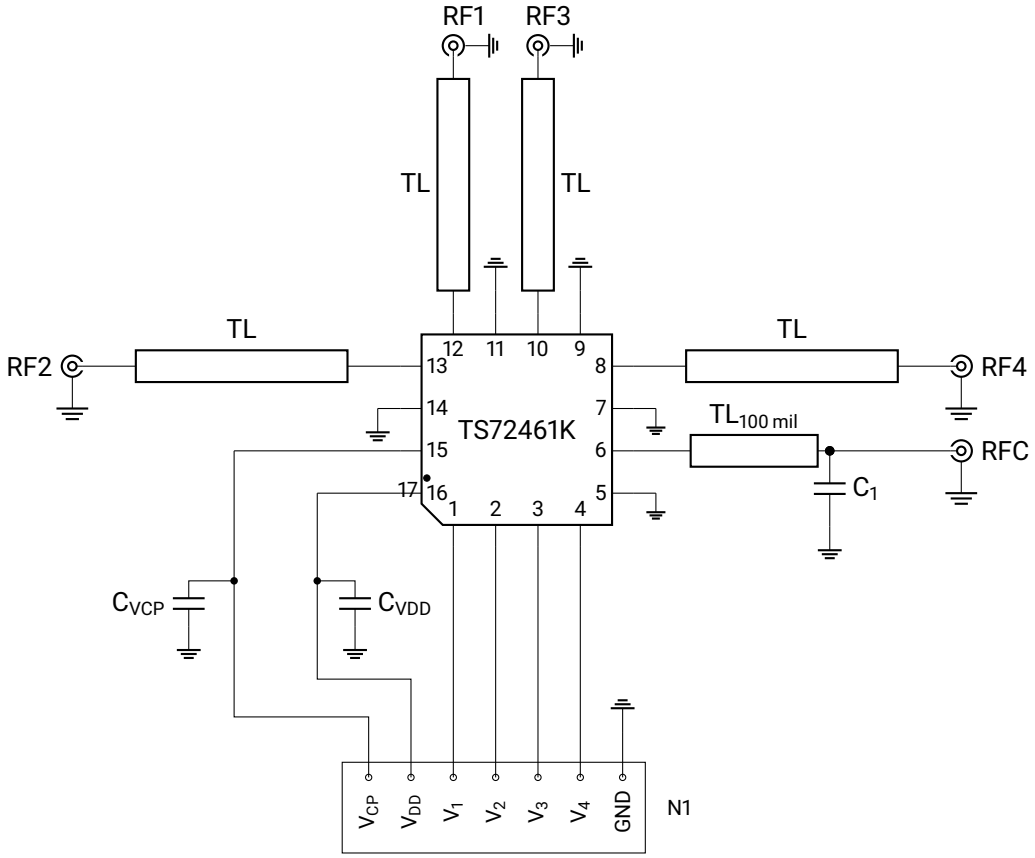
Schematics and Evaluation Board



Schematics of TS72461K EVB, matched for 3.3 to 3.8 GHz

Notes:

- Pin 17 is the center pad of the device.
- The purpose of the connection between V_{CP} and connector N1 is to monitor V_{CP}, do not apply an external voltage to V_{CP}.
- For operation without matching (Typical characteristics, unmatched), C_1 is not mounted.

Table 8: Components used for TS72461K EVB, 3.3 to 3.8 GHz

Reference	Part number / Value	Description	Notes
$TL_{100\ mil}$	50 Ω, 100 mil	Transmission line	Between RFC pin and C_1
C_1	0.5 pF	Ceramic capacitor	Passive Plus, 0603N series
C_{VDD}	10 nF	Capacitor	
C_{VCP}	1 nF	Capacitor	

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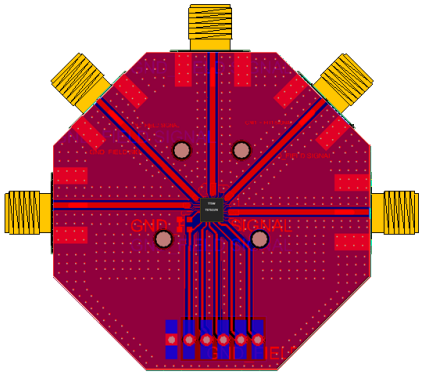

TS72461K EVB

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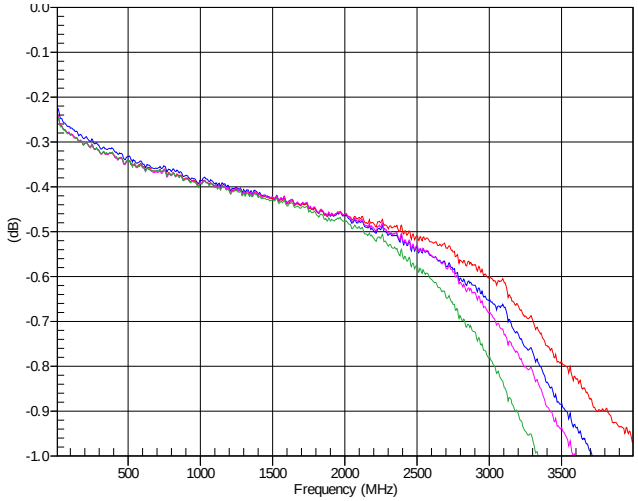
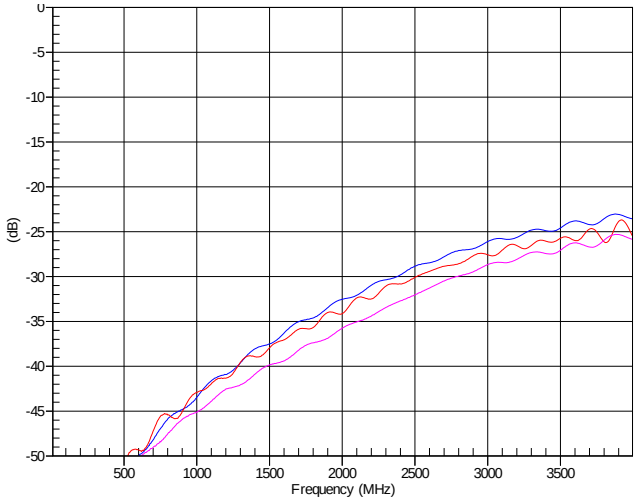
Typical characteristics

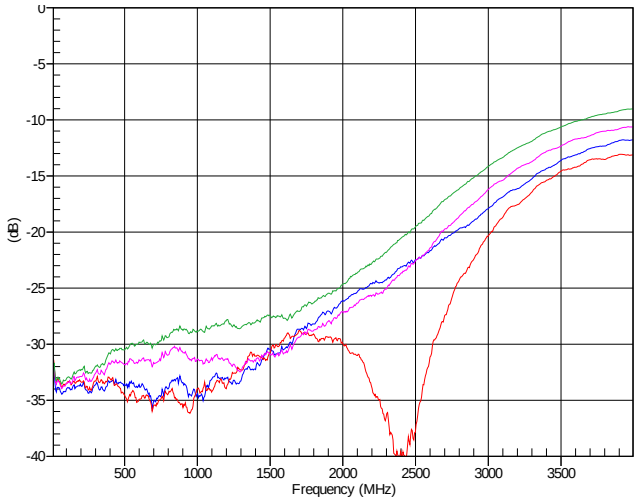
Performance, unmatched



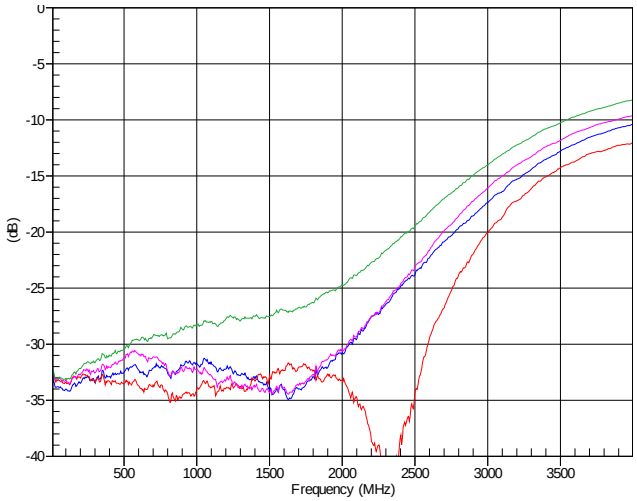
RF1 to RF4 insertion loss



RF1 ON, isolation to RF2 to RF4



RF1 to RF4 return loss



RFC return loss

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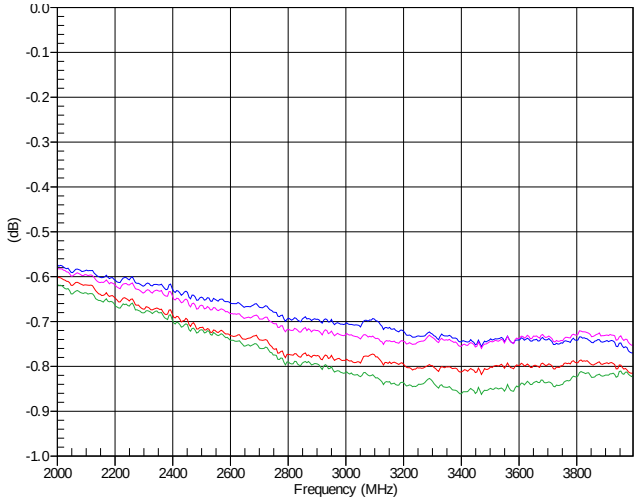
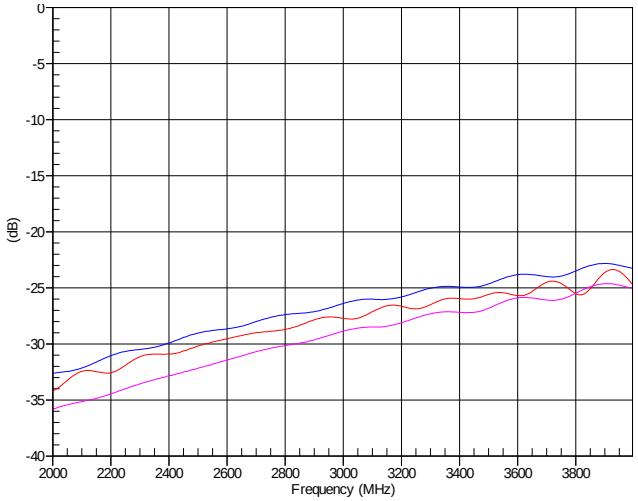
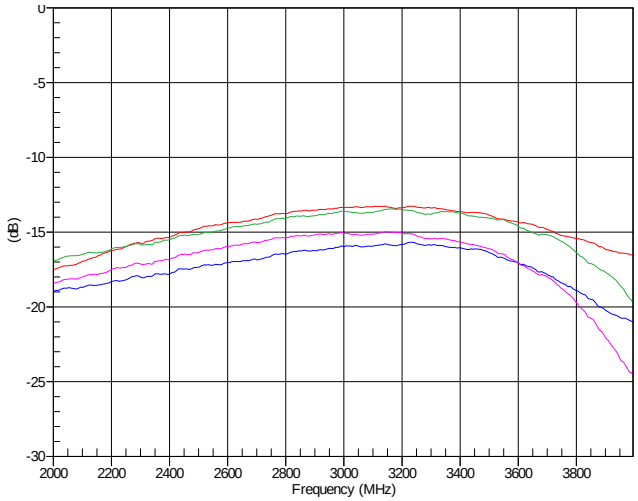
Performance, matched for 3.3 to 3.8 GHz



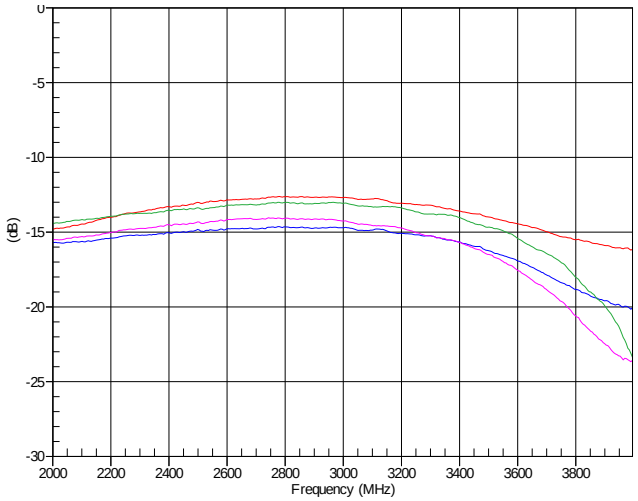
RF1 to RF4 insertion loss



RF1 ON, isolation to RF2 to RF4



RF1 to RF4 return loss



RFC return loss

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Device Package information

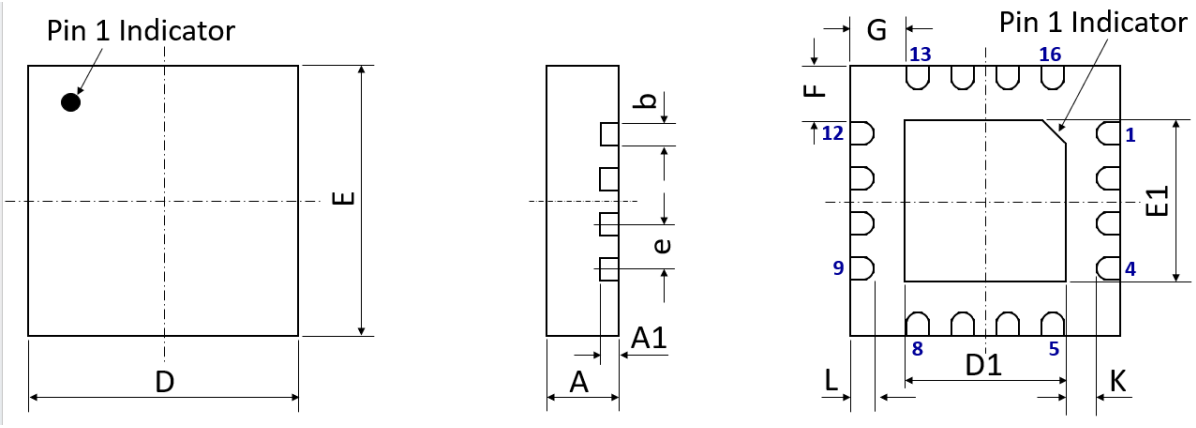

Figure 8: 16-pin QFN 3.0 x 3.0 x 0.75 mm^3 package drawing.

Please refer to application notes TN-001 PCB Design guideline and TN-002 Solder Rework at TagoreTech web page for PCB and soldering guidelines.

Table 9: Device Package Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A	0.75	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Lead finish: pure Sn without underlayer; thickness 7.5 μm to 20 μm (typical 10 μm to 12 μm).

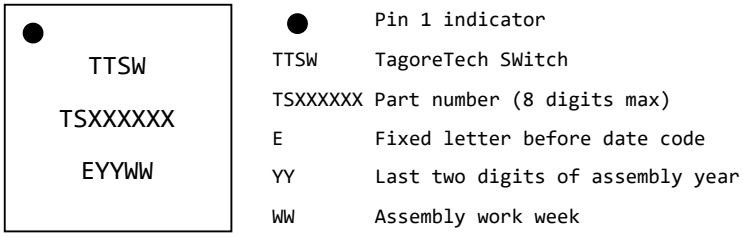

Figure 9: Part marking specification.

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PCB Land Design

Notes:

- 4-layer PCB is recommended.
- Via diameter is recommended to be 0.2 mm to prevent solder wicking inside the vias.
- Thermal vias shall only be placed on the center pad.
- The maximum via number for the center pad is 3(X)×3(Y)=9.

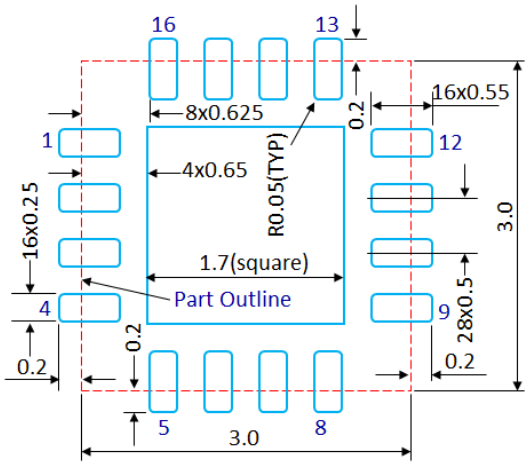

Figure 10: PCB land pattern, dimensions in [mm].



Figure 11: Solder mask pattern, non-solder mask defined (preferred, left) and solder mask defined (right), dimensions in [mm].

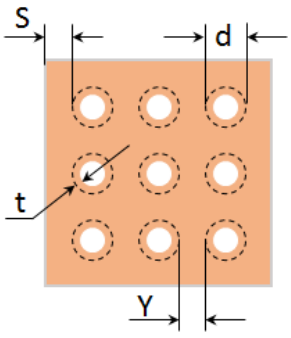

Figure 12: Thermal Via Pattern, Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm.

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PCB Stencil Design

Notes:

- Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- Stencil thickness is recommended to be 125μm.

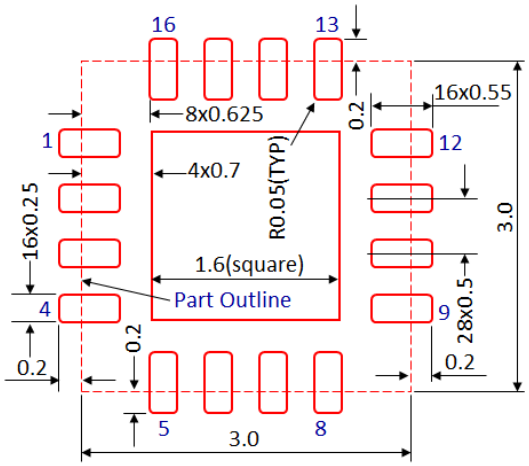

Figure 13: Stencil Openings, dimensions in [mm].

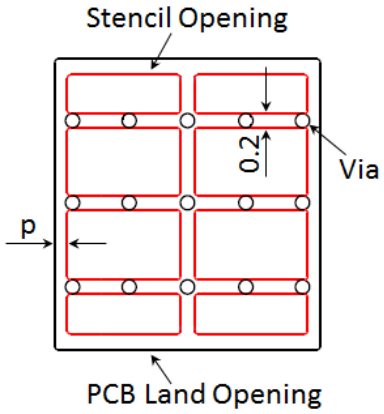

Figure 14: Stencil Openings Shall not Cover Via Areas If Possible, dimensions in [mm].

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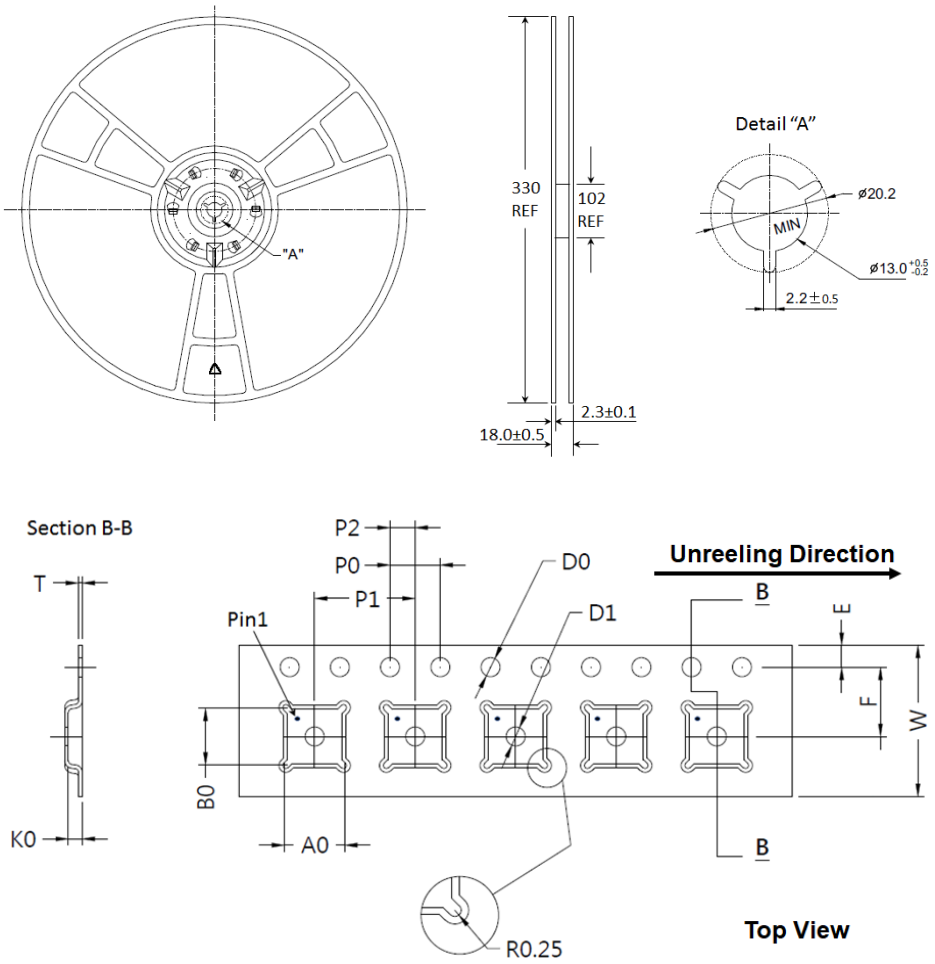
Tape and Reel Information



A0[mm]	B0[mm]	D0[mm]	D1[mm]	E[mm]	F[mm]	K0[mm]	P0[mm]	P1[mm]	P2[mm]	T[mm]	W[mm]
3.35	3.35	1.50	1.50	1.75	5.50	1.10	4.00	8.00	2.00	0.30	12.00

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Glossary

IL	Insertion loss
ISO	Isolation
RL	Return loss
VSWR	Voltage Standing Wave Ratio
RFC	RF Common port, sometimes referred to as ANT
RFx	RF Port number x
V_x	Control input of throw RFx

Changelog

Table 10: Changelog

Date	Revision	Notes
08/27/2024	2.0	Previous datasheet revision (Word).
11/01/2026	3.00	Transferred to the TagoreTech datasheet format. New functional diagram and pin assignment drawing with series and shunt switches, switch state diagrams, V_{DD} off state, package height 0.75 mm, return loss shown as negative values, EVB schematic redrawn, links to application notes TN-001/TN-002, QR code link to the latest datasheet, glossary.

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