SPDT 100 W_{peak} Asymmetric GaN RF Switch 500 MHz to 5.0 GHz

Features

- Frequency Range 500 MHz to 5.0 GHz
- Low insertion loss (TX/RX): 0.40 dB/0.60 dB @ 2.6 GHz
- High isolation (RX path): 40 dB @ 2.6 GHz
- High peak power handling capability
- No external DC blocking capacitors on RF lines
- All RF ports OFF state
- Versatile 2.6 V – 5.5 V power supply

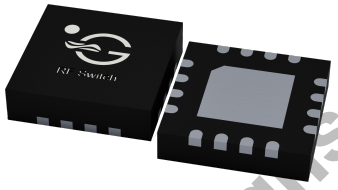

Figure 1: TS7329K in 3.0 x 3.0 mm^2 QFN 16-pin package.

Applications

- 4G, 5G systems
- RX protection
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Radar

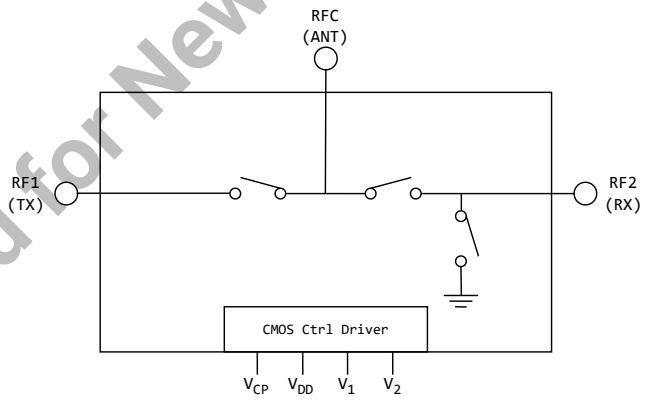

Figure 2: TS7329K functional diagram

General Description

The TS7329K is an asymmetrical reflective Single Pole Double Throw (SPDT) switch designed for broadband, high peak power switching applications. Its broadband behavior from 500 MHz to 5.0 GHz makes the TS7329K an excellent switch for all applications requiring low insertion loss, high isolation, and high linearity within a small package size.

The TS7329K is housed in a compact 3.0×3.0 mm^2 16-lead Quad Flat No-lead (QFN) plastic package.

RoHS

RoHS10/REACH/Halogen free

Not Recommended for New Designs

For new designs, please consider TagoreTech **TS8329K** (TS8329K datasheet).

Scan for the TS8329K datasheet

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Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TS7329K	16 Pin 3.0x3.0x0.75 mm^3 QFN	Core part number
TS7329K-EVB	Evaluation Board	
TS7329KMTRPBF[1]	330 mm reel, 3 000 pcs	Full reel

[1] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	13” (330mm)	18mm

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Pin Assignment

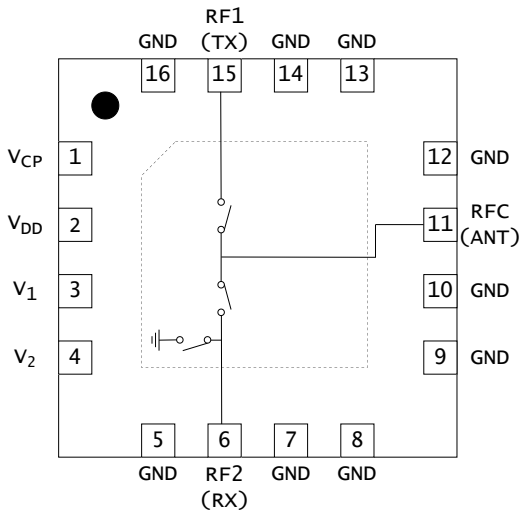

Figure 3: TS7329K pin assignment [top view]

Table 3: Pin Definition

Pin Number	Pin Name	Description
1	V_{CP}	Internal charge pump voltage output, connect a 1 nF capacitor to GND on this pin to improve switching time.
2	V_{DD}	DC Power Supply
3	V_1	Switch control input 1
4	V_2	Switch control input 2
5	GND	Ground
6	RF2(RX)	RF2 (RX) port
7,8,9,10,12,13,14,16	GND	Connect to ground[2]
11	RFC(ANT)	RF Common (Antenna) port
15	RF1(TX)	RF1 (TX) port
17 [1]	GND	Ground thermal pad, please connect to GND

[1] The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.
[2] These pins are NC pins inside the package. To avoid floating pins around RF lines, we request these to be connected to ground.

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	V_{DD}	5.5	V
External bias voltage on V_{CP} pin	V_{CP}	-20	V
Storage Temperature Range	T_{st}	−55 – 125	°C
Operating Temperature Range	T_{op}	−40 – 85	°C
Maximum Junction Temperature	T_j	+140	°C
Maximum RF CW input power, 800 MHz, T_J=+85°C	$TX-ANT$	42	dBm
Maximum RF CW input power, 800 MHz, T_J=+105°C	$TX-ANT$	41	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	25	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta jt}$	36	°C/W
Soldering Temperature	T_{solder}	+260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 – $<$1000	V
Charged Device Model (CDM)	Level C3	$\geq$1000	V
Moisture Rating			
Moisture Sensitivity Level[2]	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and can cause permanent damage to the device. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.

[2] Tagore recommends to store parts in moisture barrier bag to preserve solderability.

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Electrical Specifications

Table 5: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency[1]	f	500		5000	MHz
Insertion loss, TX	800 MHz		0.30	0.40	dB
$ANT - TX$	1.95 GHz		0.35	0.45	dB
	2.6 GHz		0.40	0.55	dB
	3.8 GHz		0.40		dB
	5.0 GHz (matched)[2]		0.45		dB
Insertion loss, RX	800 MHz		0.50	0.65	dB
$ANT - RX$	1.95 GHz		0.55	0.70	dB
	2.6 GHz		0.60	0.75	dB
	3.8 GHz		0.70		dB
	5.0 GHz (matched)[2]		0.85		dB
Isolation	800 MHz	39	42		dB
$ANT - TX$	1.95 GHz	30	33		dB
	2.6 GHz	27	30		dB
	3.8 GHz		27		dB
	5.0 GHz (matched)[2]		23		dB
Isolation	800 MHz	52	55		dB
$ANT - RX$	1.95 GHz	42	45		dB
	2.6 GHz	37	40		dB
	3.8 GHz		35		dB
	5.0 GHz (matched)[2]		30		dB
Return Loss	800 MHz		-30		dB
$ANT - TX, RX$	1.95 GHz		-25		dB
	2.6 GHz		-23		dB
	3.8 GHz		-22		dB
	5.0 GHz (matched)[2]		-18		dB
Isolation @ Peak Power	P_{peak}=49.2 dBm, ISO RX @3.8 GHz		35		dB

[1] No external DC blocking capacitors are required on RF pins unless DC voltage is applied on a RF pin.
[2] With the 4.4 – 5 GHz matching capacitor described in the Schematics and Evaluation Board section.

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Table 6: Electrical Specifications $T_A = +25°C; V_{DD} = +3.3V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	500		5000	MHz
Harmonic Distortion					
H_2	800MHz, P_{in} =35dBm		-75		dBc
H_3	800MHz, P_{in} =35dBm		-80		dBc
IIP3	800MHz		70		dBm
Power and Compression point					
$P_{0.1dB}$ TX[2]	700 MHz – 3.8 GHz, CW	42			dBm
$P_{peak0.1dB}$ TX[3]	700 MHz – 3.8 GHz, pulsed power	49.2	50		dBm
$P_{0.1dB}$ RX[2]	700 MHz – 3.8 GHz, CW	39			dBm
Switching Time					
t_{SW}, $C_{VCP} = 1nF$	50% ctrl to 10/90% settled RF value		0.35		μs
Power Supply, DC					
Control voltage	Power Supply V_{DD}	2.6	3.3	5.5	V
	All control pins high[4], V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control current	All control pins high, I_{ih}			7.5	μA
	All control pins low, I_{il}		0		μA
Current consumption	I_{DD}, active mode (V_{DD} on)		160	200	μA

[2] $P_{0.1dB}$ is a figure of merit. Please do not exceed Absolute Maximum ratings.
[3] Peak power was verified with 1% duty cycle and 10 μs pulse width.
[4] Control voltage V_{ih} cannot be higher than V_{DD} (to avoid forward biasing of ESD diode)

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Switching time definition

Example of the definition by using 10 W/40 dBm signal. We apply 10W signal to RF port, stabilized with isolator. Isolator is needed as our switch shows to RF port approximately 4Ω impedance. Let's assume that the switch insertion loss is 0.3 dB. Therefore 90% of the RF signal is 39.55 dBm and 10% of the RF signal is 1W/30dBm. We need to take into account 0.3dB insertion loss, therefore numbers are 39.25 dBm and 29.7 dBm respectively. We change the control from low to high and our time reference point is when our control signal exceeds lower threshold value V_{ihlow}. In certain measurements when control signal rise time is significantly shorter than RF output signal, we approximate start of the clock with 50% point of the control signal.

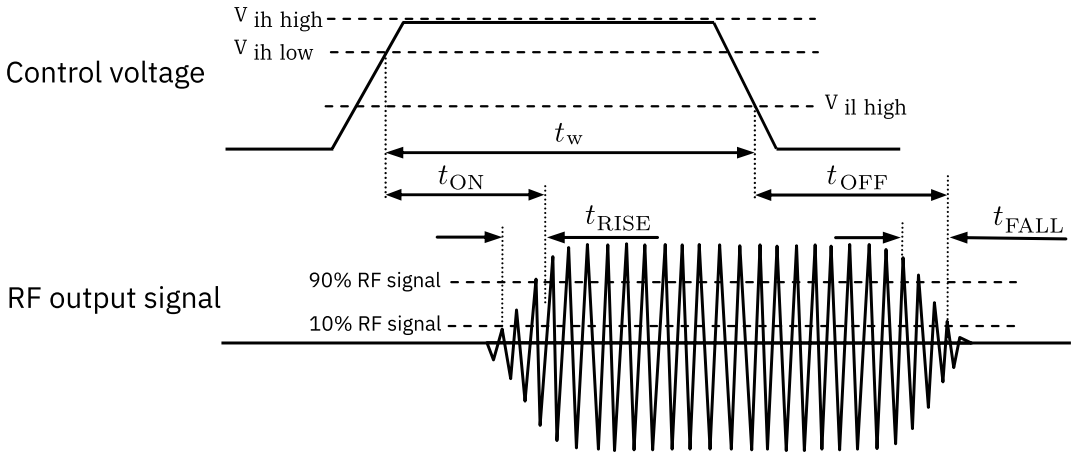

Figure 4: Switching time definition, t_{ON}, t_{OFF}, t_{RISE}, t_{FALL}. Minimum pulse width t_w.

Our component uses integrated charge pump. Maximum pulse repetition rate defines what is maximum frequency for switching events. Please do not exceed given maximum frequency. By feeding external -18 V to V_{CP}, one can improve maximum pulse repetition rate f_{PRR}. Feeding external -18V to V_{CP}, one can drive switch at least to 20kHz f_{PRR}. Expect current consumption of 10mA of -18V.

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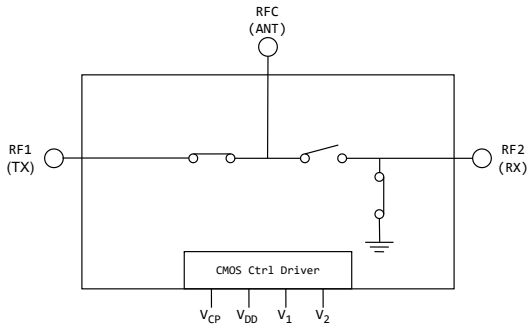
Switch Control table

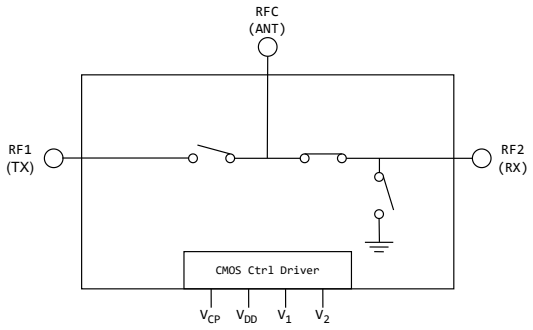
Table 7: Switch Control Table

V_{DD}[1]	V_2	V_1	**Switch state**
1	0	0	$RFC(ANT) - RF1(TX)$ ON[2]
1	0	1	$RFC(ANT) - RF2(RX)$ ON
1	1	0	ISO State[3]
0	0	0	V_{DD} OFF State[3]

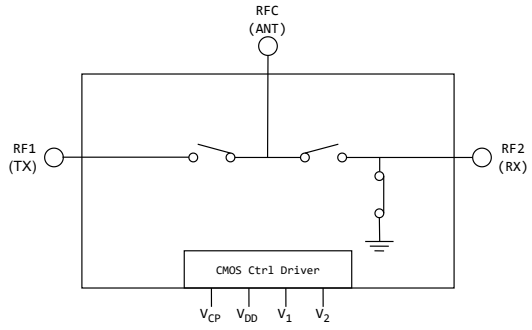
[1] V_{DD} should be applied first before V_1 and V_2, otherwise may cause damage to the device.
[2] There are internal pull-downs to ground on both V_1 and V_2 control pins, the state at start-up without any control voltage applied will be $ANT - TX$ ON.
[3] If All OFF state is not used, the switch can be operated with single control pin V_1



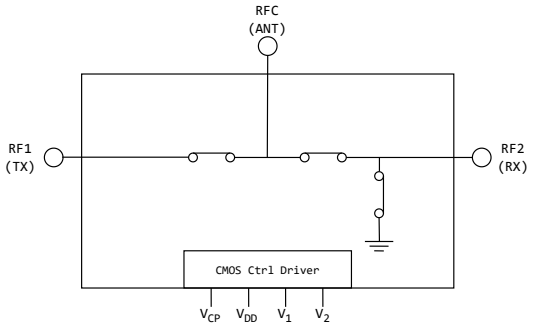
RFC-RF1 ON



RFC-RF2 ON



ISO (Isolation state)



V_{DD} off state

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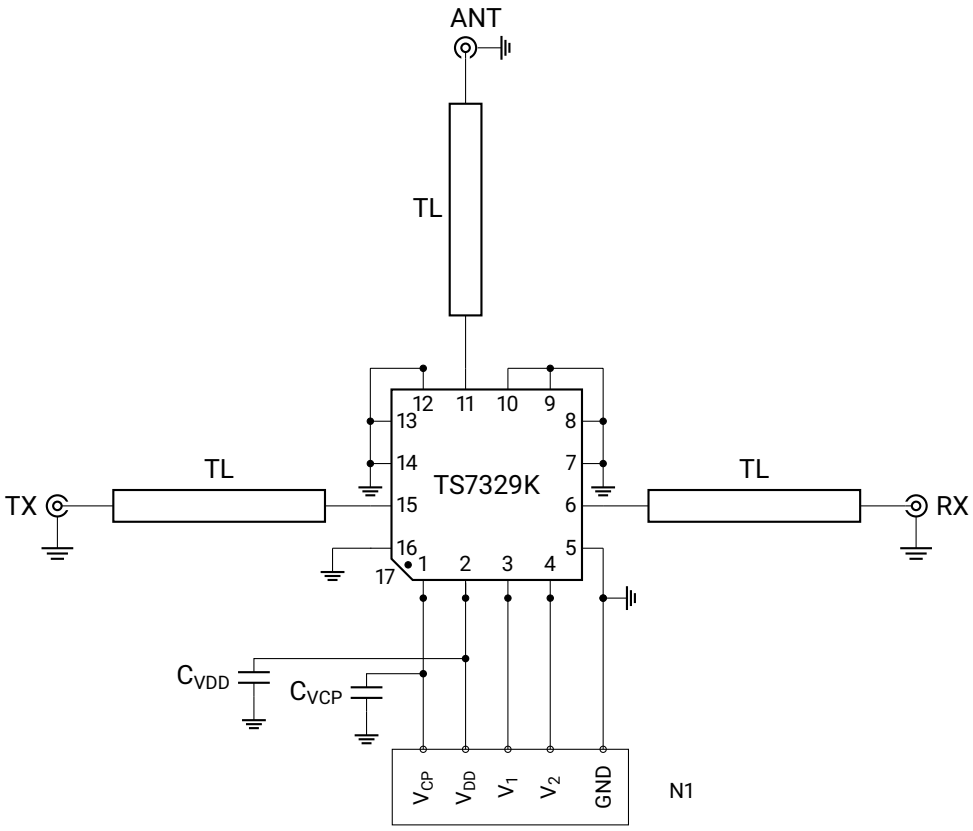
Theory of Operation

Feeding external V_{CP} voltage of -18 V

TS7329K supports external voltage supply to V_{CP} to increase pulse repetition rate f_{PRR}. With external voltage supply, f_{PRR} can be increased at least to support pulse repetition rate more than 20 kHz, in some cases even up to 100 kHz. In order to use external voltage, it is mandatory to supply first V_{DD}, have a delay of 1 ms and then apply -18 V to V_{CP}. Shutdown should be in opposite order.

Schematics and Evaluation Board

Only two external components are recommended, 1 nF for V_{CP} and 10 nF for V_{DD} lines. Pin 17 in the schematic refers to the center (thermal) pad of the device. Below 4 GHz, no matching is required on the ANT port. For 4.4 – 5 GHz operation, add a shunt 0.3 pF capacitor (Passive Plus 0402N0R3AW251) to GND, as close as possible to the RFC (ANT) pin.



Schematics of TS7329K EVB

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Table 8: Components used for TS7329K EVB

Reference	Part number / Value	Description	Notes
C_{VDD}	10nF	Capacitor	
C_{VCP}	1nF	Capacitor	
C_{match}	0402N0R3AW251	Ceramic capacitor (Passive Plus)	0.3 pF, shunt at ANT pin, for 4.4 – 5 GHz matching

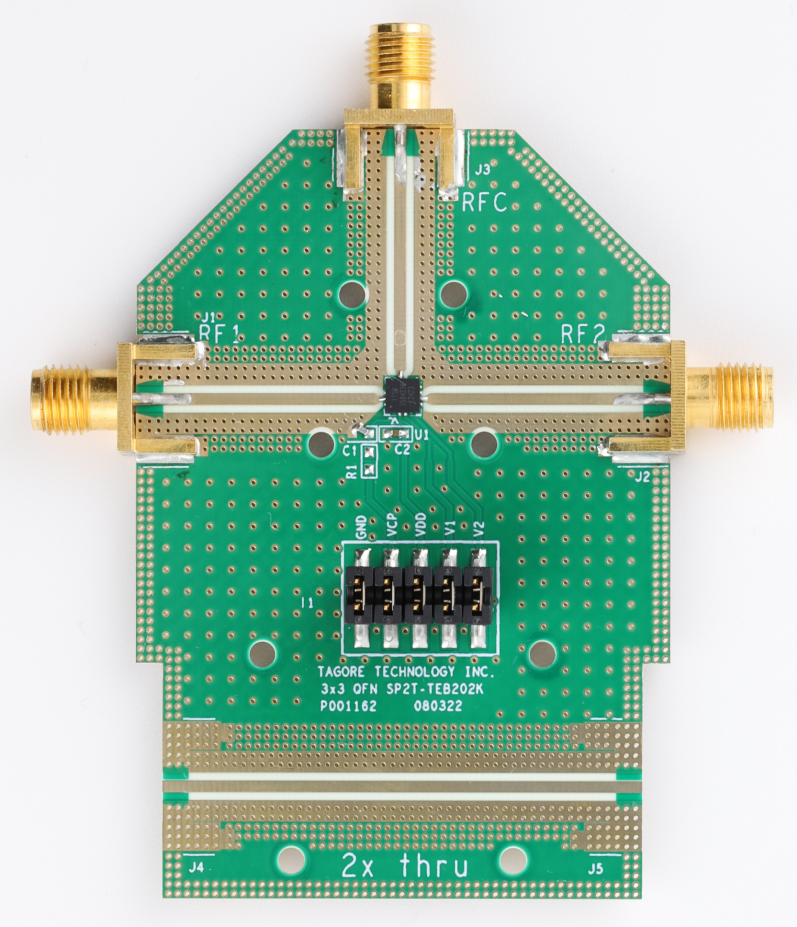

Photo of TS7329K EVB

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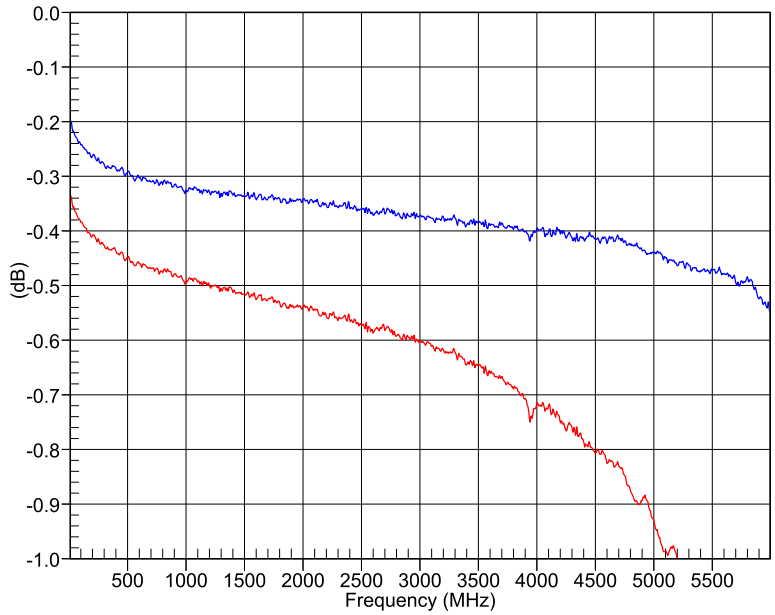
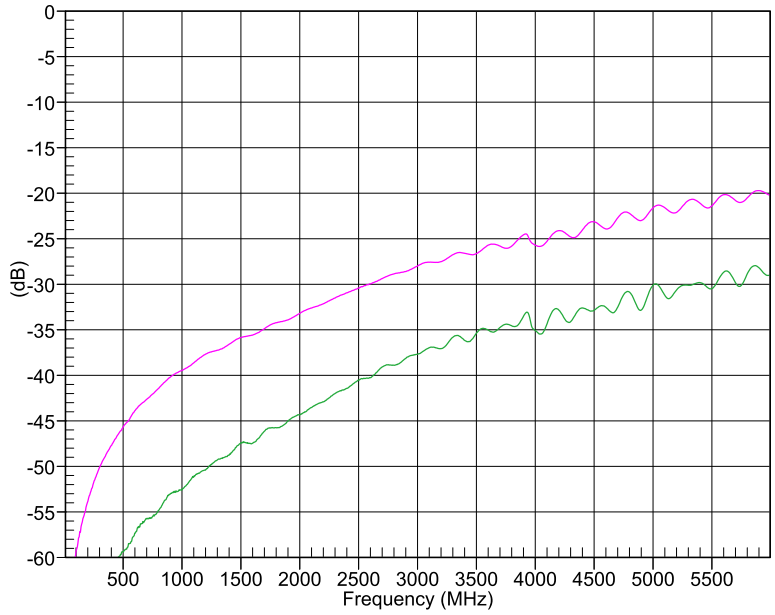
Typical characteristics

These measurements have been taken from TS7329K EVB.

With no match



TX, RX Insertion loss.



TX, RX Isolation.

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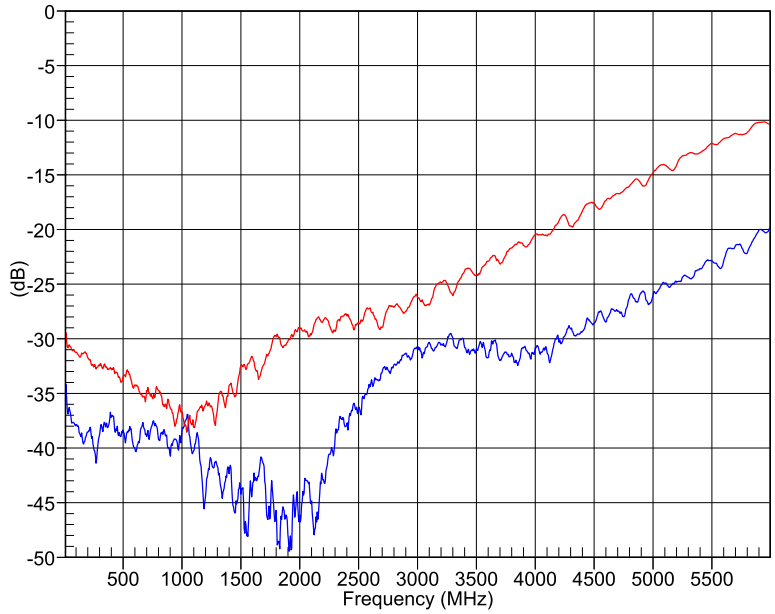
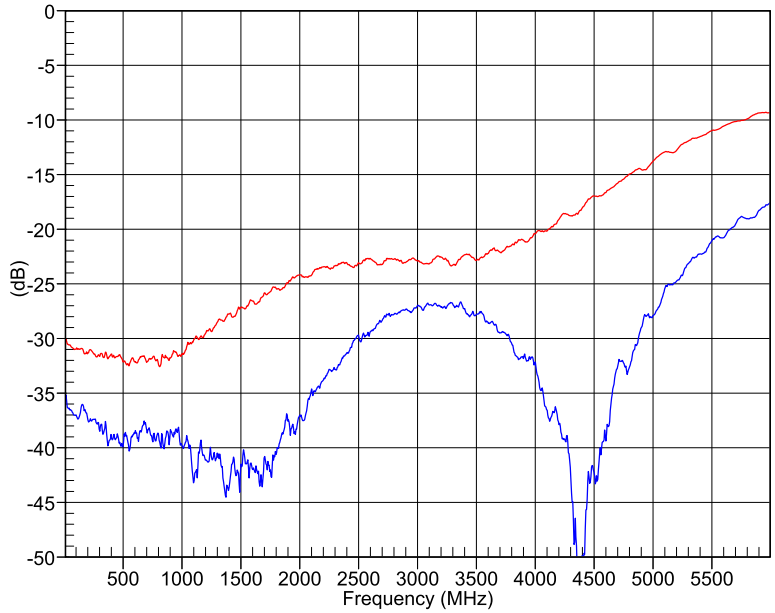


TX, RX Return loss.



RFC (ANT) Return loss.

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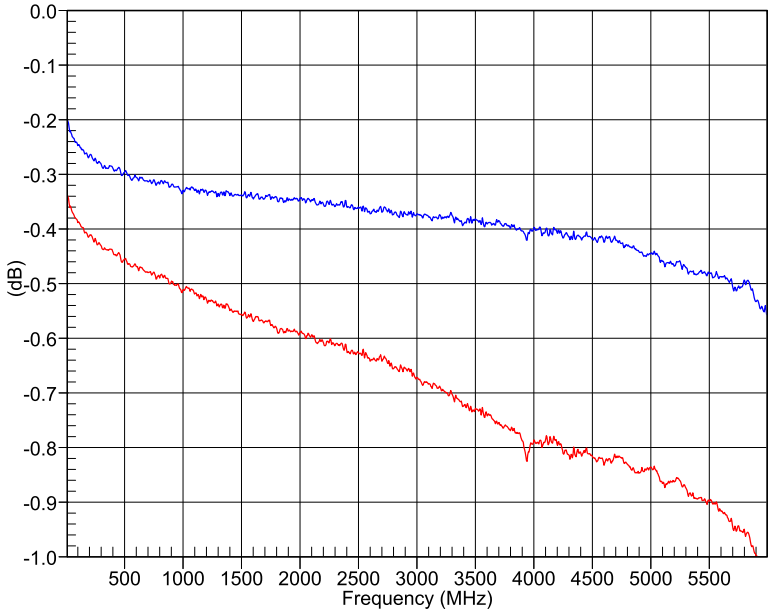
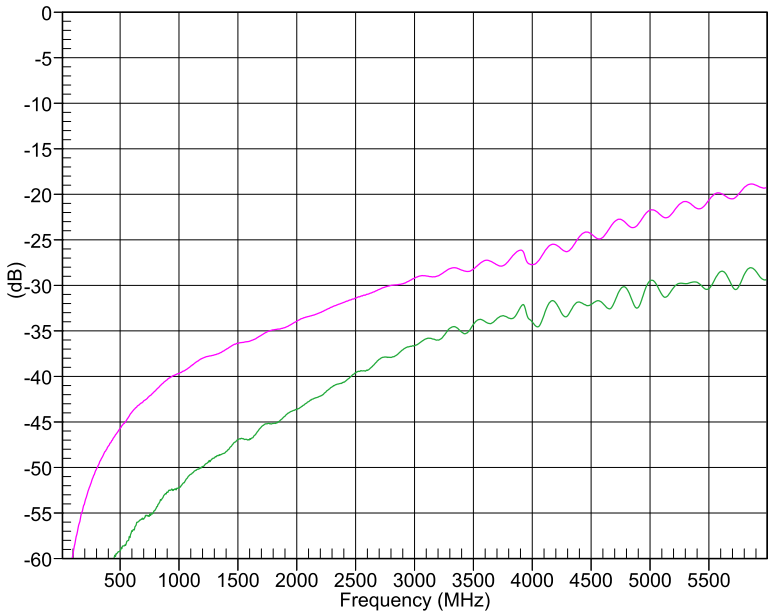
With match tuned for 4.4 – 5 GHz



TX, RX Insertion loss.



TX, RX Isolation.

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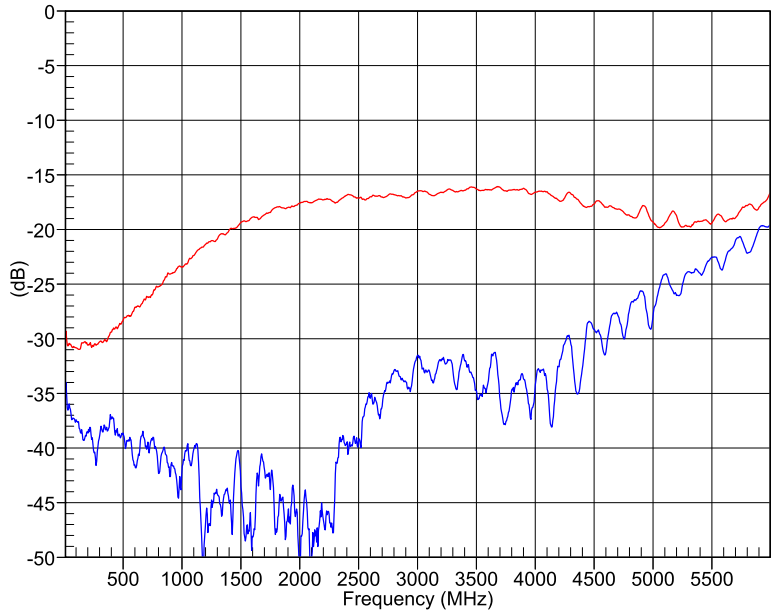
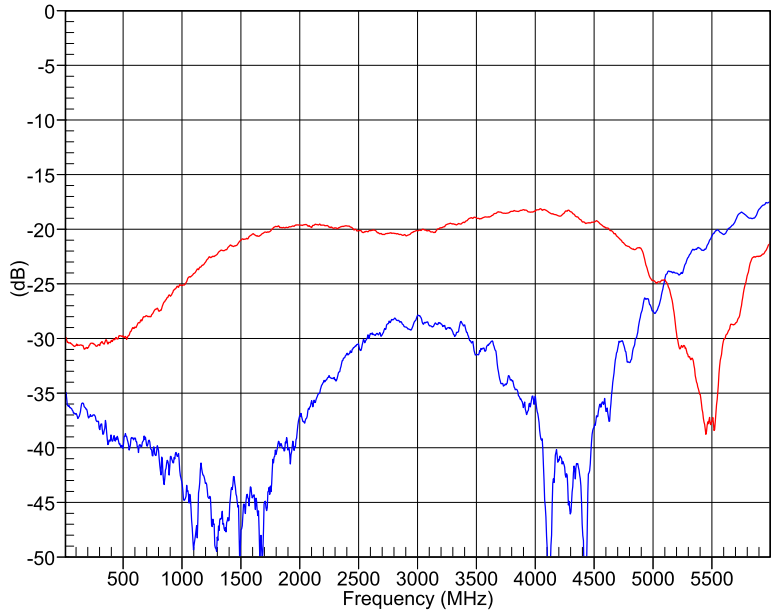


TX, RX Return loss.



RFC (ANT) Return loss.

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Device Package information

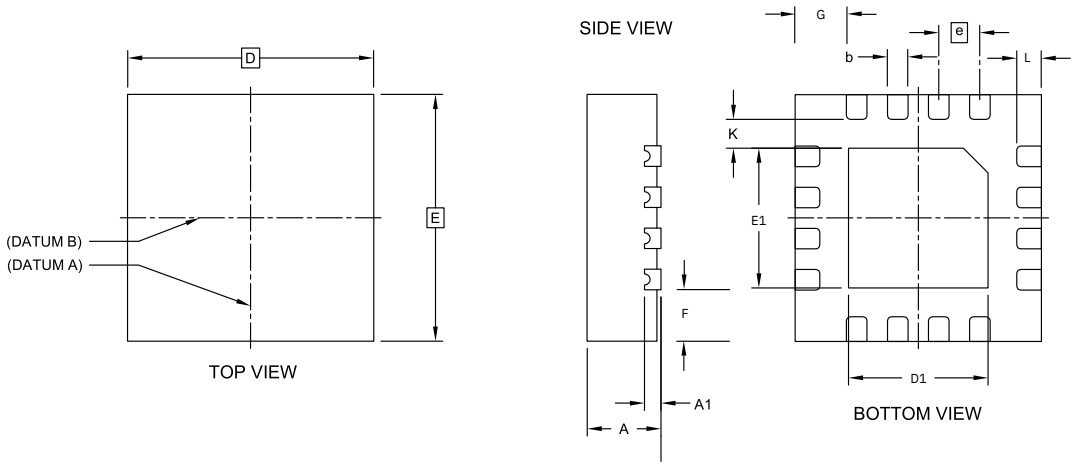

Figure 6: 16-pin QFN 3.0 x 3.0 x 0.75 mm^3 package drawing.

Please refer to application notes TN-001 PCB Design guideline and TN-002 Solder Rework at TagoreTech web page for PCB and soldering guidelines.

Table 9: Device Package Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A	0.75	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	±0.05	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Lead finish: Pure Sn without underlayer; thickness 7.5 μm – 20 μm (typical 10 – 12 μm).

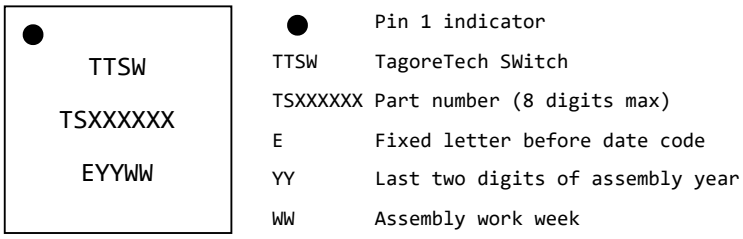

Figure 7: Part marking specification.

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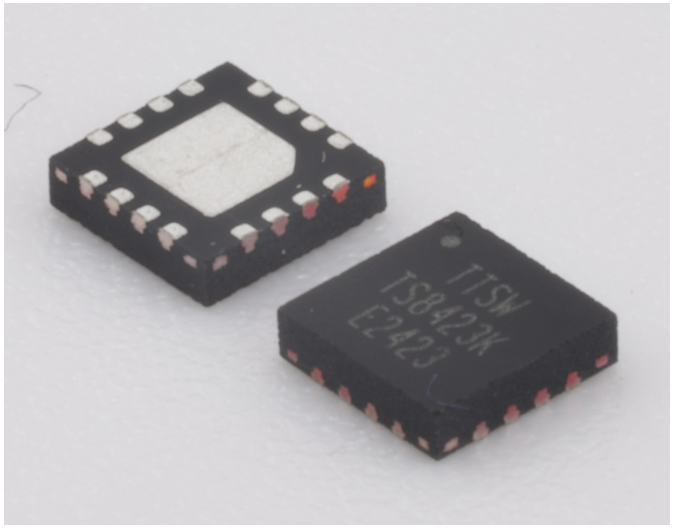

Figure 8: TS7329K photo, top and bottom side.

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PCB Land Design

Notes:

- 4-layer PCB is recommended.
- Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
- Thermal vias shall only be placed on the center pad.
- The maximum via number for the center pad is 3(X)×3(Y)=9.

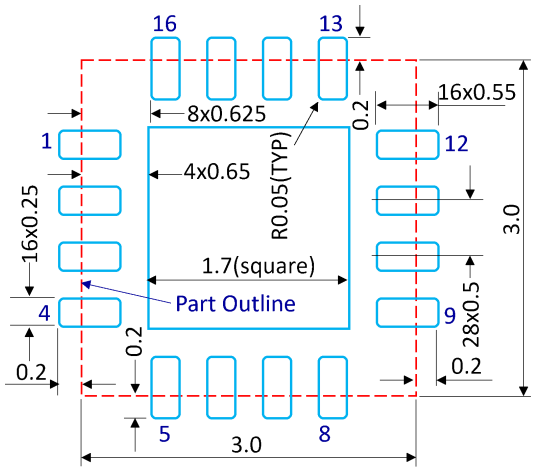

Figure 9: PCB land pattern, dimensions in [mm].

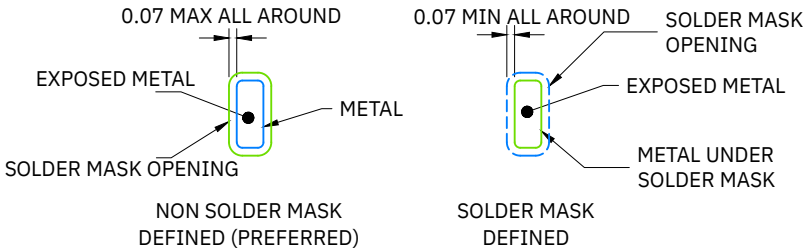

Figure 10: Solder mask opening, dimensions in [mm].

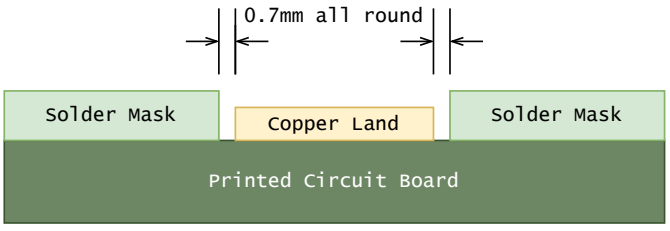

Figure 11: Preferred solder mask opening, side view, dimensions in [mm].

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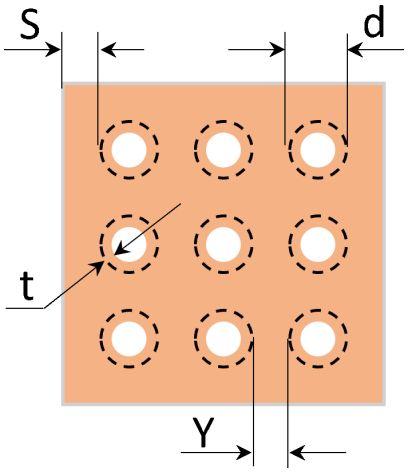

Figure 12: Thermal Via Pattern, Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm.

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PCB Stencil Design

Notes:

- Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- Stencil thickness is recommended to be 125μm.

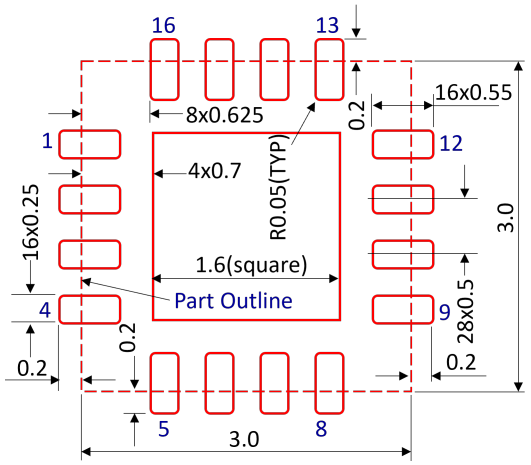

Figure 13: Stencil Openings, dimensions in [mm].

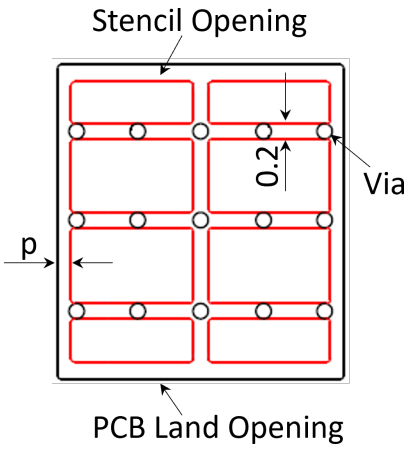

Figure 14: Stencil Openings Shall not Cover Via Areas If Possible, dimensions in [mm].

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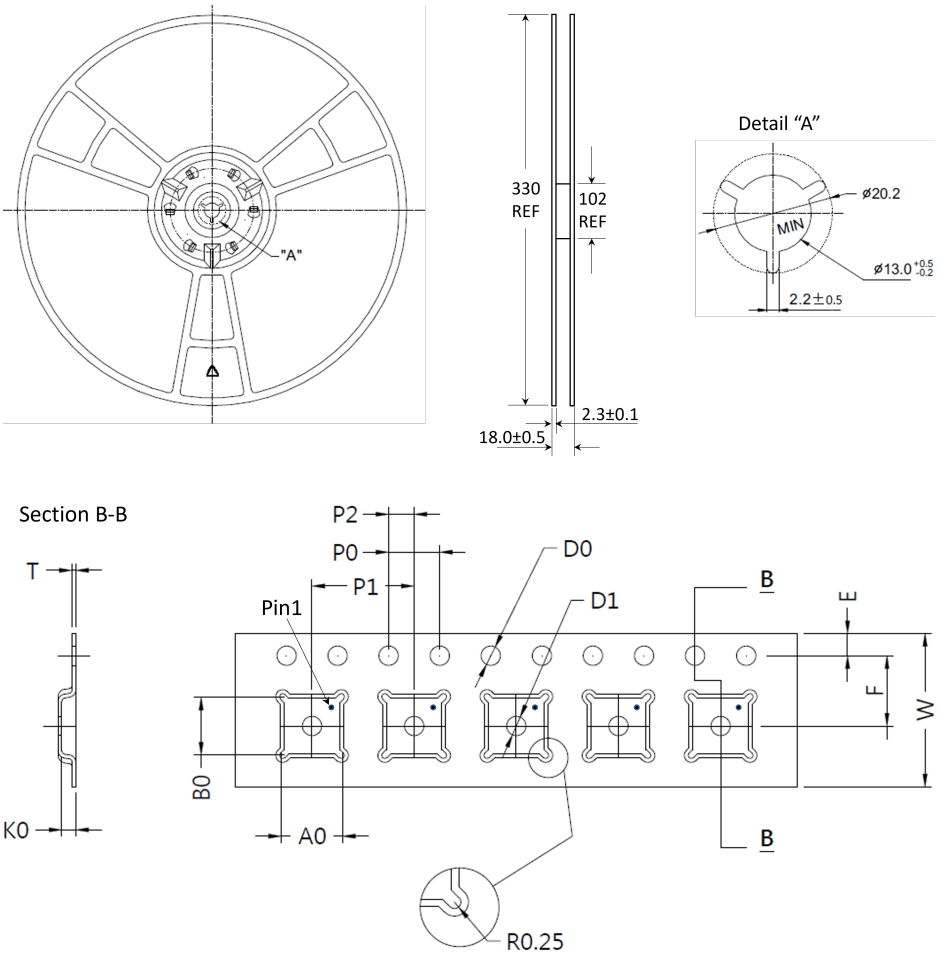
Tape and Reel Information



A0[mm]	B0[mm]	D0[mm]	D1[mm]	E[mm]	F[mm]	K0[mm]	P0[mm]	P1[mm]	P2[mm]	T[mm]	W[mm]
3.35	3.35	1.50	1.50	1.75	5.50	1.10	4.00	8.00	2.00	0.30	12.00

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Glossary

IL	Insertion loss
ISO	Isolation
RL	Return loss
VSWR	Voltage Standing Wave Ratio
ANT	Antenna port or common port, sometimes referred as RFC
TX	Transmit port
RX	Receive port

Changelog

Table 10: Changelog

Date	Revision	Notes
08/28/2024	2.4	TS7329K datasheet, previous format.
09/23/2026	3.00	Datasheet converted to common TagoreTech datasheet template, package thickness corrected to 0.75mm, V_{CP} absolute maximum rating added, marked Not Recommended for New Designs (replacement part TS8329K).

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