30 W CW GaN Broadband RF Switch SPDT (Obsolete)

Features

- Low insertion loss: 0.30 dB @ 800 MHz
- High isolation: 44 dB @ 800 MHz
- High linear power handling capability
- No external DC blocking capacitors on RF lines
- Versatile 2.6 V – 5.5 V power supply

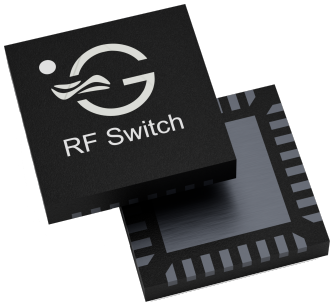

Figure 1: TS7421L in 4.0 x 4.0 mm^2 QFN 32-pin package.

Applications

- Private mobile radio handsets
- Public safety handsets
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals

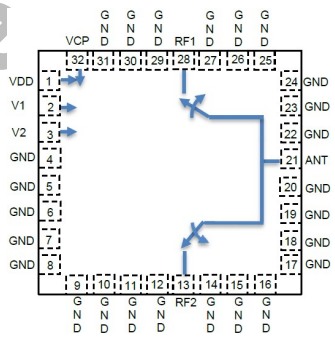

Figure 2: TS7421L functional diagram [top view]

General Description

The TS7421L is a symmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high peak power switching applications. Its broadband behavior from 500 MHz to 5 GHz makes the TS7421L an excellent switch for all the applications requiring low insertion loss, high isolation and high linearity within a small package size.

The TS7421L is packaged into a compact Quad Flat No lead (QFN) 4.0x4.0 mm^2 32 leads plastic package.

The TS7421L is obsolete. No parts are available and there will be no further production. This document is retained for reference only. The TagoreTech TS7423L and TS8022L are suitable replacement parts with exactly the same footprint and pinout.

RoHS10/REACH/Halogen free

Obsolete

Contents

Features 1
Applications 1
General Description 1
Ordering information 3
Pin Assignment 4
Absolute Maximum Ratings 6
Electrical Specifications 7
Switch Control table 9
Evaluation Board Schematic 10
Typical characteristics 11
Device Package information 12
PCB Land Design 14
PCB Stencil Design 16
Tape and Reel Information 17
Glossary 18
Changelog . . . 18
Legal Information 19
Published by . . . 19
Legal Disclaimer . . . 19
Support Contact . . . 19
TS7421L Document information . . . 19
TagoreTech Inc. Product Brochure and datasheets . . . 19

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Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TS7421L[1]	32 Pin 4.0x4.0x0.75 mm^3 QFN	Core part number
TS7421L-EVB	Evaluation Board	
TS7421LMTRPBF[2]	330 mm reel, 3 000 pcs	Full reel

[1] The TS7421L is obsolete. No parts are available and there will be no further production; the information is retained for reference only. Suitable replacements with the same footprint and pinout: TS7423L, TS8022L.
[2] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	13” (330mm)	18mm

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Pin Assignment

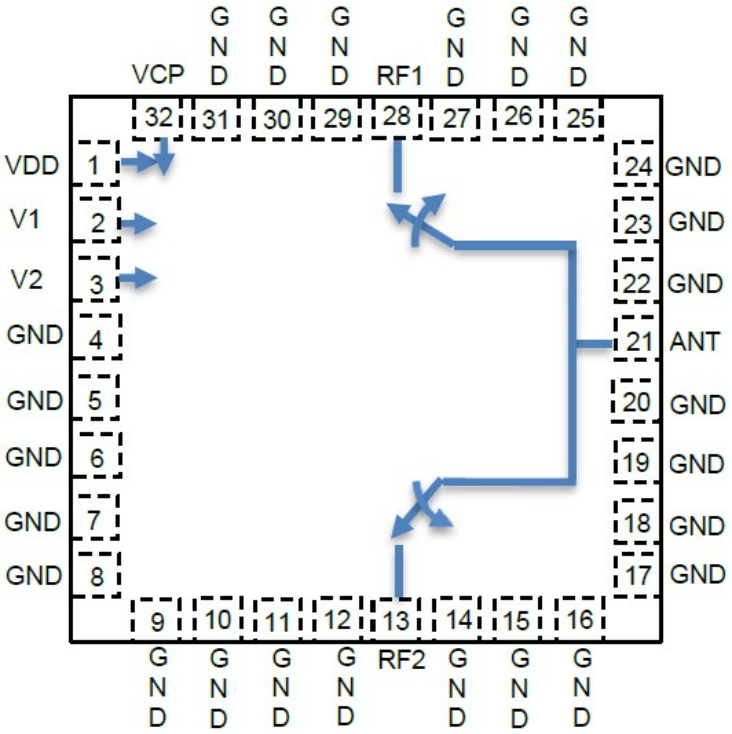

Figure 3: TS7421L pin assignment and functional diagram [top view]

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Table 3: Pin Definition

Pin Number	Pin Name	Description
1	V_{DD}	DC power supply
2	V_1	Switch control input 1
3	V_2	Switch control input 2
4,5,6,7,8,9,10,11,12,14, 15,16,17,18,19,20,22,23, 24,25,26,27,29,30,31	NC	No internal connection, can be grounded
13	RF2	RF port 2
21	ANT	Antenna port
28	RF1	RF port 1
32	V_{CP}	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.
33 [1]	GND	Ground thermal pad, please connect to GND

[1] The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management. Adequate heatsinking is required.

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	V_{DD}	2.6 – 5.5	V
External bias voltage on V_{CP} pin	V_{CP}	-20	V
Storage Temperature Range	T_{st}	−55 – 125	°C
Operating Temperature Range	T_{op}	−40 – 85	°C
Maximum Junction Temperature	T_j	+140	°C
Maximum RF CW input power, 500 – 3000 MHz, $T_C = +85$°C	RFx	45	dBm
Maximum RF CW input power, 500 – 3000 MHz (VSWR 10:1), 1 minute	RFx	44	dBm
Maximum RF CW input power, >3 GHz – 5 GHz, $T_C = +85$°C	RFx	42.5	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	10	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta jt}$	≤37	°C/W
Soldering Temperature	T_{solder}	+260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 – <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level[2]	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and can cause permanent damage to the device. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.

[2] Tagore recommends to store parts in moisture barrier bag to preserve solderability.

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Electrical Specifications

Table 5: Electrical Specifications $T_A = +25$°C unless otherwise specified; $V_{DD} = +2.7V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	500		5000	MHz
Insertion loss	500 MHz		0.30		dB
$ANT - RFx$	800 MHz		0.30	0.4	dB
	1.95 GHz		0.35	0.5	dB
	2.6 GHz		0.40	0.55	dB
	5.0 GHz		0.75		dB
Isolation	500 MHz		48		dB
$ANT - RFx$	800 MHz	40	44		dB
	1.95 GHz	32	35		dB
	2.6 GHz	28	32		dB
	5.0 GHz		22		dB
Return loss	500 MHz		-35		dB
$ANT - RFx$	800 MHz		-35		dB
	1.95 GHz		-30		dB
	2.6 GHz		-27		dB
	5.0 GHz		-17		dB

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Table 6: Electrical Specifications $T_A = +25$°C unless otherwise specified; $V_{DD} = +2.7V$; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	500		5000	MHz
Harmonic Distortion					
H_2	800MHz, P_{in} =38dBm		-83		dBc
H_3	800MHz, P_{in} =38dBm		-80		dBc
IIP3	800MHz		74		dBm
Power and Compression point					
$P_{0.1dB}$[1]	0.1dB compression point, 500 MHz – 4 GHz		46		dBm
$P_{0.1dB}$[1]	0.1dB compression point, >4 GHz		45		dBm
Switching Time					
t_{SW}[3]	Switching time, C1=1nF		0.8		μs
Power Supply, DC					
Control voltage	Power Supply V_{DD}	2.6	3.3	5.5	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control current	All control pins high, I_{ih}			7.5	μA
	All control pins low, I_{il}		0		μA
Current consumption	I_{DD}, active mode (V_{DD} on)		160	200	μA

[1] $P_{0.1\,dB}$ is a figure of merit. Please do not exceed Absolute Maximum ratings.
[2] No external DC blocking capacitors are required on the RF pins unless a DC voltage is applied on a RF pin.
[3] From 50% of the control signal to 10/90% of the settled RF value. C1=1nF to GND on the V_{CP} pin (see Evaluation Board Schematic).
[4] Insertion loss goes up by 0.1 dB at $+85$°C base plate temperature.

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Switch Control table

Table 7: Switch Control Table

V_1[1]	V_2	**Active RF Path**
0	1	All OFF[2]
0	0	$ANT-RF1$ ON[4]
1	0	$ANT-RF2$ ON

[1] V_{DD} should be applied first before V_1 and V_2, otherwise may cause damage to the device.
[2] There is an internal pull-down to ground on the V_2 control pin, which can be left floating when the all OFF state is used.
[3] If the all OFF state is not used, the switch can be operated with the single control pin V_1.
[4] There is also an internal pull-down to ground on the V_1 control pin; the state at start-up without any control voltage applied will be $ANT-RF1$ ON by default.

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Evaluation Board Schematic

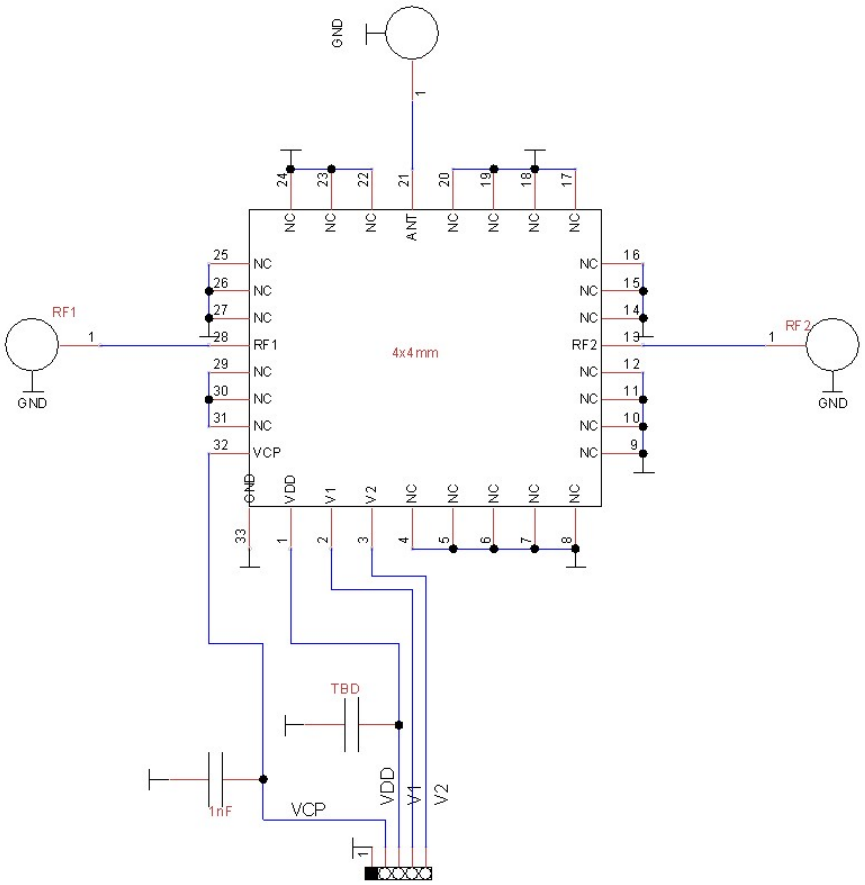

Figure 4: Evaluation board schematic.

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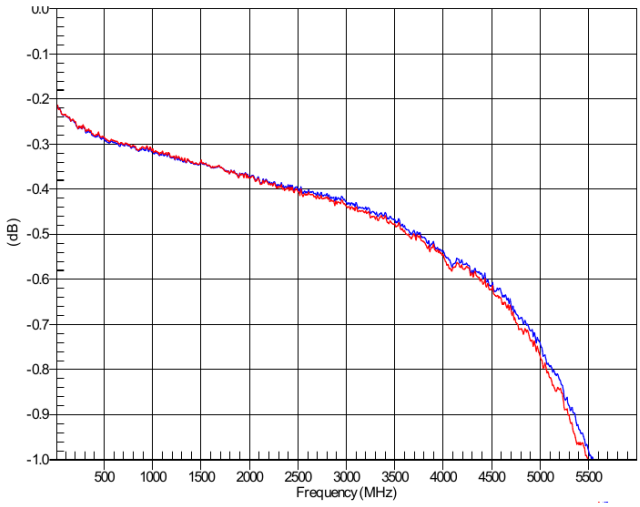
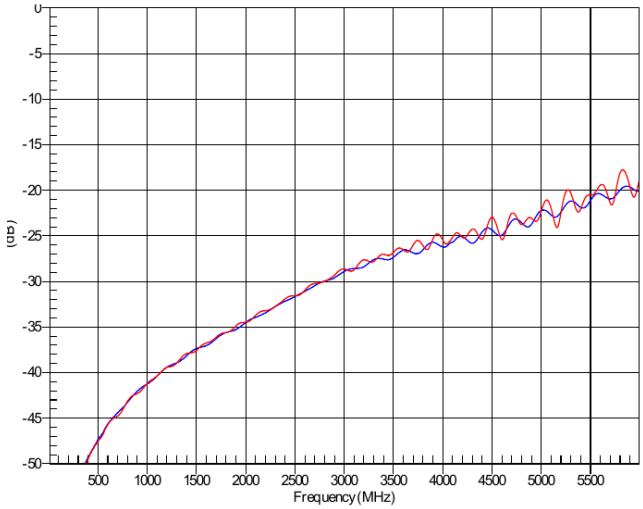
Typical characteristics

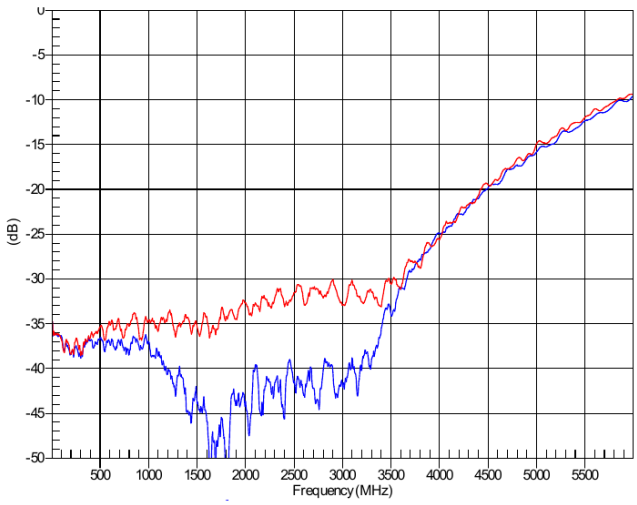
The following measurements were obtained from the TS7421L evaluation board.



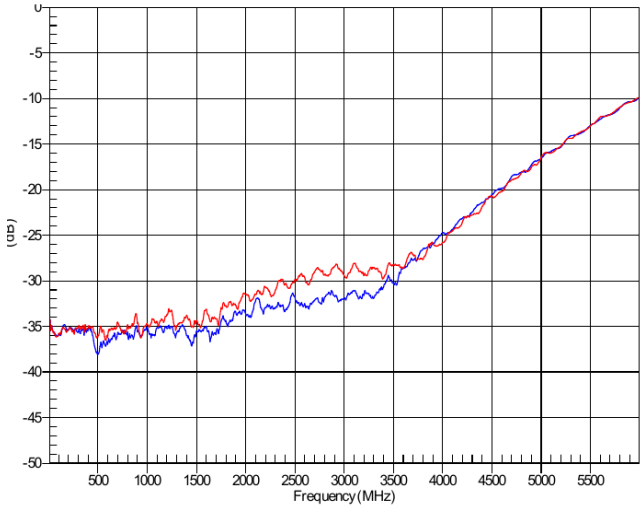
(a) RF1, RF2 insertion loss.



(b) RF1, RF2 isolation.



(a) RF1, RF2 return loss.



(b) ANT return loss.

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Device Package information

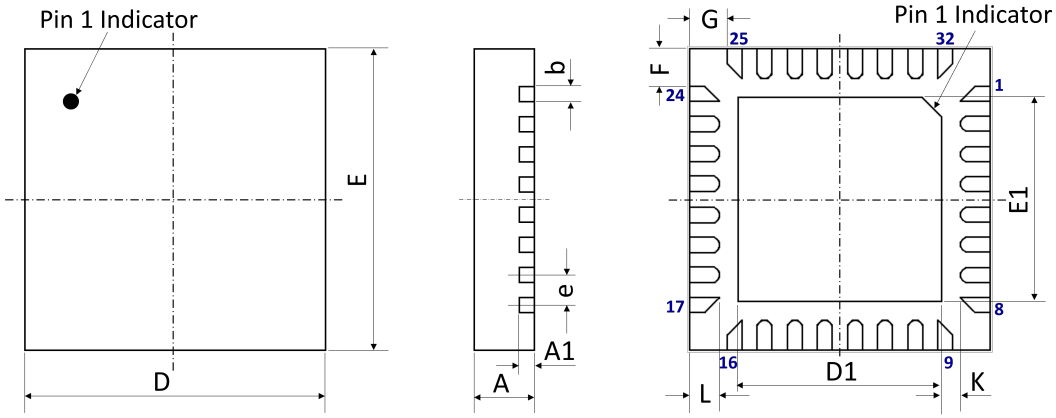

Figure 7: 32-pin QFN 4.0 x 4.0 x 0.75 mm^3 package drawing.

Please refer to application notes TN-001 PCB Design guideline and TN-002 Solder Rework at TagoreTech web page for PCB and soldering guidelines.

Table 8: Device Package Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A	0.75	±0.05	E	4.00 BSC	±0.05
A1	0.203	±0.02	E1	2.70	±0.05
b	0.20	+0.05/-0.07	F	0.50	±0.05
D	4.00 BSC	±0.05	G	0.50	±0.05
D1	2.70	±0.05	L	0.40	±0.05
e	0.40 BSC	±0.05	K	0.25	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm – 20μm (Typical 10μm – 12μm).

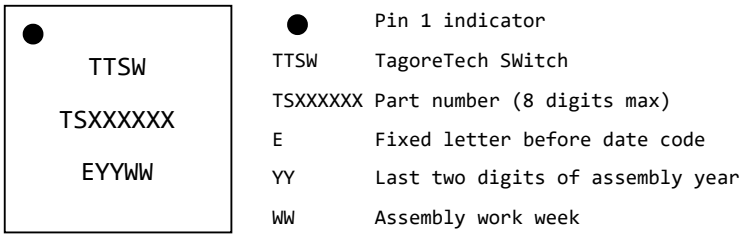

Figure 8: Part marking specification.

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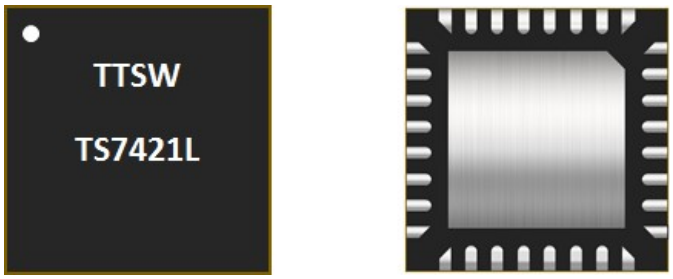

Figure 9: TS7421L photo, top side and package bottom.

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PCB Land Design

Notes:

- 4-layer PCB is recommended.
- Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
- Thermal vias shall only be placed on the center pad.
- The maximum via number for the center pad is 4(X)×4(Y)=16.

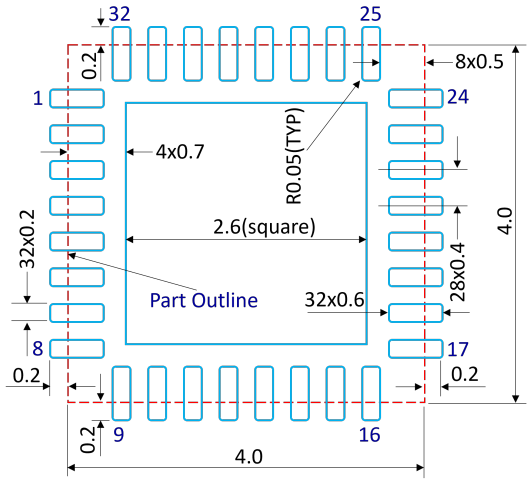

Figure 10: PCB land pattern, dimensions in [mm].

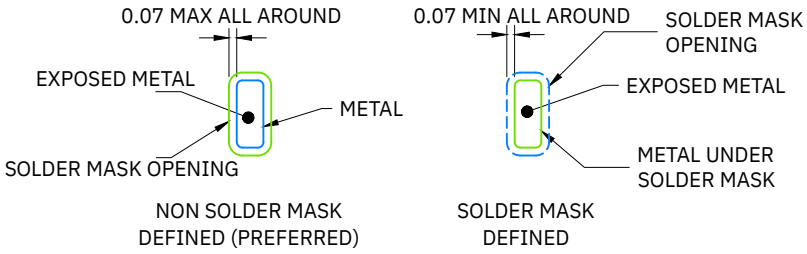

Figure 11: Solder mask opening, dimensions in [mm].

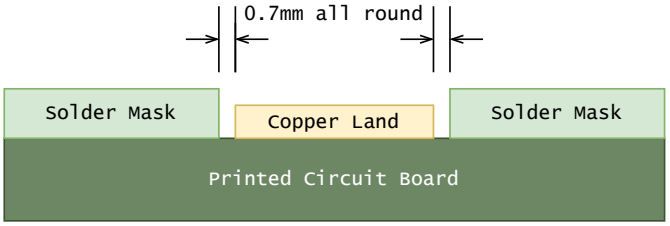

Figure 12: Preferred solder mask opening, side view, dimensions in [mm].

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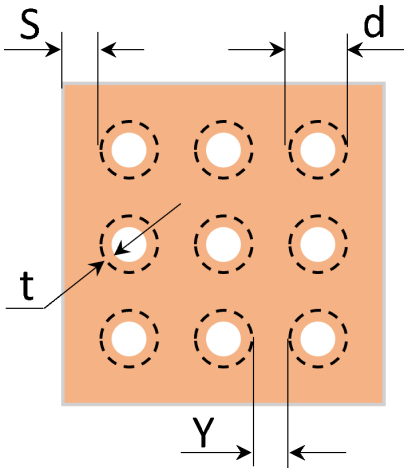

Figure 13: Thermal Via Pattern, Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm.

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PCB Stencil Design

Notes:

- Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- Stencil thickness is recommended to be 125μm.

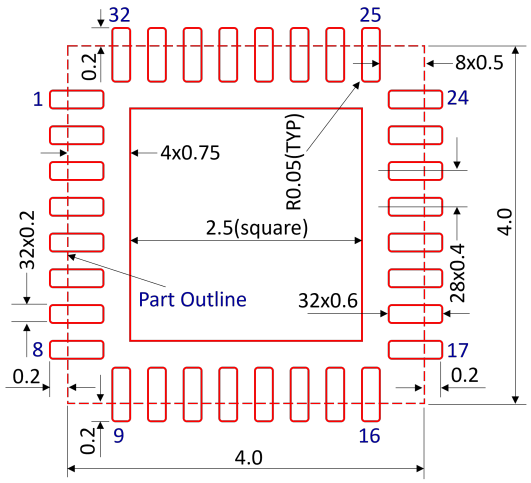

Figure 14: Stencil Openings, dimensions in [mm].

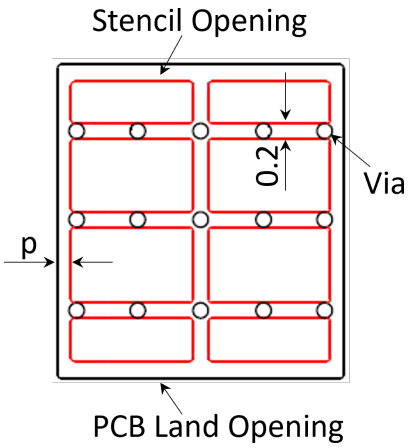

Figure 15: Stencil Openings Shall not Cover Via Areas If Possible, dimensions in [mm].

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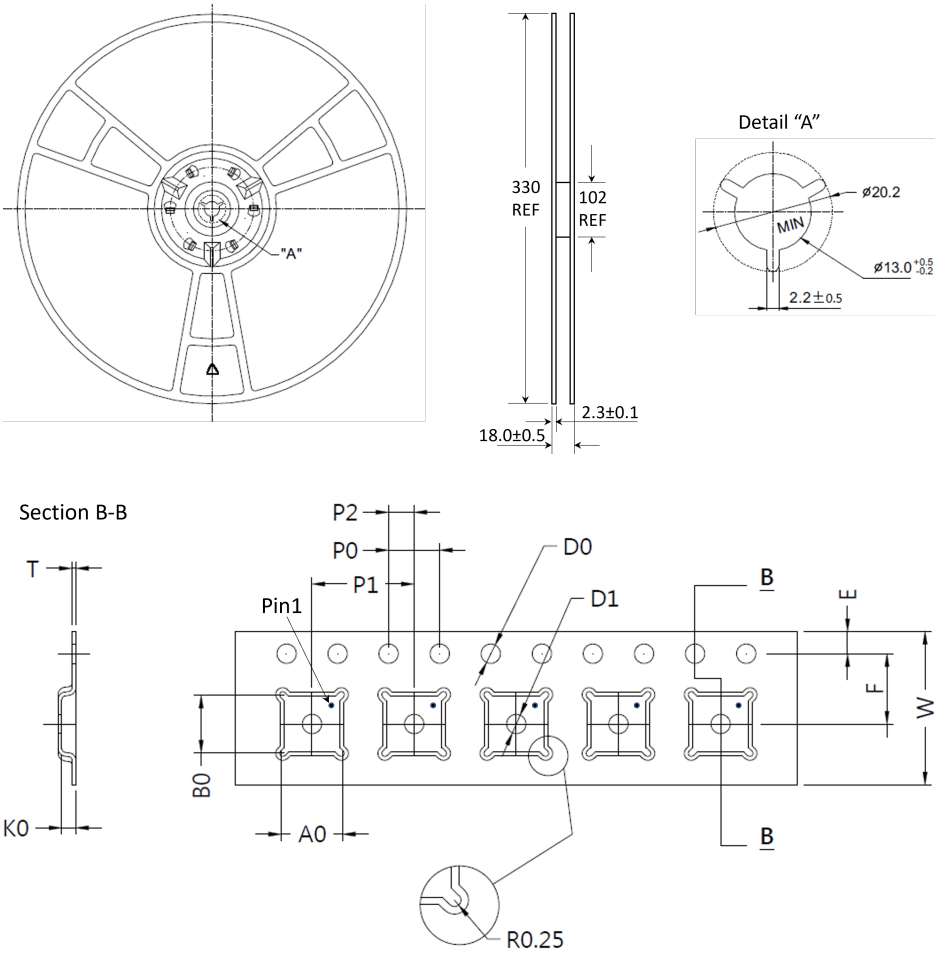
Tape and Reel Information



A0[mm]	B0[mm]	D0[mm]	D1[mm]	E[mm]	F[mm]	K0[mm]	P0[mm]	P1[mm]	P2[mm]	T[mm]	W[mm]
4.35	4.35	1.50	1.50	1.75	5.50	1.10	4.00	8.00	2.00	0.30	12.00

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Glossary

IL	Insertion loss
ISO	Isolation
RL	Return loss
SPDT	Single Pole Dual Throw
VSWR	Voltage Standing Wave Ratio
ANT	Antenna port, sometimes referred as RFC (RF Common)
RFx	RF Port number x

Changelog

Table 9: Changelog

Date	Revision	Notes
09/06/2024	2.4	Datasheet in the previous format.
09/26/2026	3.00	Final edition, for reference only: datasheet converted to the common TagoreTech document template. Obsolete markings and replacement part information (TS7423L, TS8022L) added, links to application notes TN-001/TN-002, package height corrected to 0.75mm, V_{CP} absolute maximum rating added, return loss given in house sign convention.

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Legal Information

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Support Contact

The TS7421L is obsolete: no parts are available, there will be no further production, and this document is retained for reference only. For support regarding existing designs, please contact TagoreTech:
support@tagoretech.com

For new designs, please consider the TagoreTech TS7423L (TS7423L datasheet) or TS8022L (TS8022L datasheet), which have exactly the same footprint and pinout as the TS7421L.

TS7421L Document information

This final edition of the TS7421L datasheet is available for download: TS7421L Datasheet

TagoreTech Inc. Product Brochure and datasheets

Tagore Product Brochure and links to all available datasheets is available for download

TagoreTech Product Brochure