SPDT 550 W_{pulse}/631 W_{peak} T/R Switch 0.5 GHz to 2.0 GHz

Features

- Frequency Range 500 MHz to 2.0 GHz
- Low TX insertion loss:
  0.27 dB @ 915 MHz
  0.25 dB @ 1200 MHz – 1310 MHz (matched)
- High RX isolation:
  52 dB @ 915 MHz
  47 dB @ 1200 MHz – 1310 MHz (matched)
- 550 W_{pulse}, 20 % duty cycle, 2.0 ms pulse width
- At least 631 W_{peak} (58 dBm), 1 % duty cycle, LTE/5G
- Switching time 1.4 µs
- Tuning inductor pins for an isolation notch
- Low power consumption, less than 1 mW
- No external DC blocking capacitors on RF lines
- Versatile 2.6 V – 5.5 V power supply
- No need to supply negative voltages

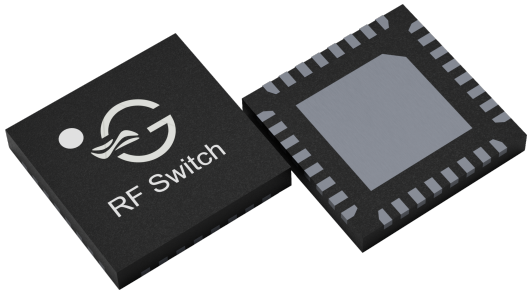

Figure 1: TS8729N in 5.0 x 5.0 mm^2 QFN 32-pin package.

Applications

- L-band radar
- High-power transmit/receive transceivers
- Tactical radios
- LTE and 5G transmit/receive switching

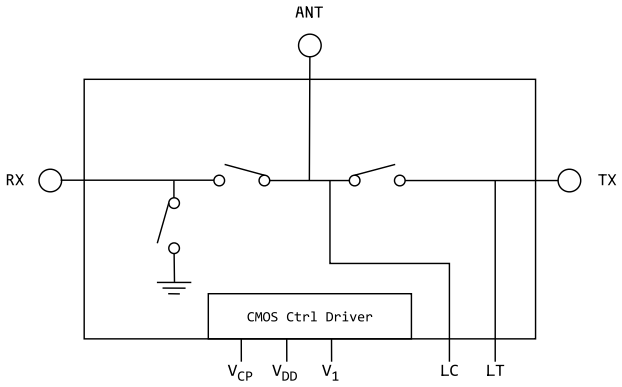

Figure 2: TS8729N functional diagram

General Description

The TS8729N is an asymmetrical reflective Single Pole Double Throw (SPDT) GaN switch designed for high-power transmit/receive switching. The TX branch has a series switch only, which gives low insertion loss and high power handling, and the RX branch has a series and a shunt switch, which gives high isolation from ANT to RX in transmit mode. The TS8729N covers 500 MHz to 2.0 GHz and handles 550 W pulse power with 20 % duty cycle and 2.0 ms pulse width; the peak power capability is at least 631 W (58 dBm) with 1 % duty cycle, for example with LTE and 5G signals. An external tuning inductor between pins 17 and 18 creates a notch in the isolation curve. No negative supply voltage or external RF DC-blocking capacitors are required.

The TS8729N is housed in a compact 5.0×5.0 mm^2 32-lead Quad Flat No-lead (QFN) plastic package.

RoHS

RoHS10/REACH/Halogen free

Contents

Features 1
Applications 1
General Description 1
Ordering information 3
Pin Assignment 4
Absolute Maximum Ratings 5
Electrical Specifications 6
Switching time definition . . . 8
Switch Control table 9
Theory of Operation 10
Asymmetrical switch topology . . . 10
Tuning inductor and isolation notch . . . 10
V_{DD} off state . . . 10
Application Information 10
Schematics and Evaluation Board 11
Unmatched EVB (IDX00), up to 1.0 GHz . . . 12
Matching example (IDX01), 1200 to 1310 MHz . . . 14
Typical characteristics 15
Performance up to 2.0 GHz, unmatched (IDX00) . . . 15
Performance 1200 to 1310 MHz, matched (IDX01) . . . 17
Switching time . . . 19
Device Package information 20
PCB Land Design 22
PCB Stencil Design 23
Tape and Reel Information 24
Glossary 25
Changelog . . . 25
Legal Information 26
Published by . . . 26
Legal Disclaimer . . . 26
Sales Contact . . . 26
Buy TS8729N directly . . . 26
TS8729N Product Information . . . 26
TagoreTech Inc. Product Brochure and datasheets . . . 26

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Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TS8729N	32-Pin 5.0x5.0x0.75 mm^3 QFN	Core part number
TS8729N-EVB	Evaluation Board	
TS8729NMTRPBF[1]	330 mm reel, 3 000 pcs	Full reel

[1] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	13” (330mm)	18mm

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Pin Assignment

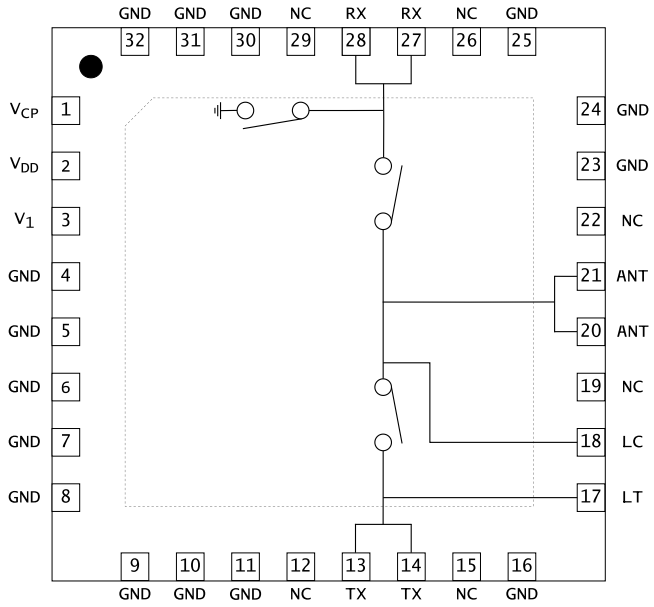

Figure 3: TS8729N pin assignment [top view]

Table 3: Pin Definition

Pin Number	Pin Name	Description
1	V_{CP}	Internal charge pump voltage output, connect a 100 nF capacitor to GND on this pin.
2	V_{DD}	DC Power Supply
3	V_1	Switch control input
13, 14	TX	TX port, please connect together
20, 21	ANT	Antenna port (RF common port), please connect together
27, 28	RX	RX port, please connect together
17	LT	Tuning inductor connection, TX side of the TX series switch[3]
18	LC	Tuning inductor connection, ANT side of the TX series switch[3]
12, 15, 19, 22, 26, 29	NC	No internal connection. Do not connect, not even to ground: needed for wider clearance and creepage distance
4–11, 16, 23–25, 30–32	GND	Connect to ground[2]
33 [1]	GND	Ground thermal pad, please connect to GND

[1] The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.
[2] These pins are NC pins inside the package. To avoid floating pins around RF lines, we request these to be connected to ground.
[3] An external inductor L_T between pins 17 and 18 creates a notch in the isolation curve, see Theory of Operation. Leave pins 17 and 18 open when the tuning inductor is not used.

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	V_{DD}	5.5	V
External bias voltage on V_{CP} pin	V_{CP}	-20	V
Storage Temperature Range	T_{st}	−55 – 125	°C
Operating Temperature Range	T_{op}	−40 – 85	°C
Maximum Junction Temperature	T_j	+140	°C
RF input power CW, $T_{case} = +85$°C, 915 MHz	TX / ANT	200 (53 dBm)	W
RF input power peak, $T_{case} = +85$°C, 915 MHz, 1 % duty cycle, 10 μs pulse width	TX / ANT	631 (58 dBm)	W
RF input power CW, $T_{case} = +85$°C, 915 MHz	RX / ANT	10 (40 dBm)	W
RF input power peak, $T_{case} = +85$°C, 915 MHz, 1 % duty cycle, 10 μs pulse width	RX / ANT	15 (41.8 dBm)	W
RF input power pulse, $T_{case} = +85$°C, 915 MHz, 20 % duty cycle, 2.0 ms pulse width	RX / ANT	12 (40.8 dBm)	W
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	3.0	°C/W
Soldering Temperature	T_{solder}	+260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 – <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level[2]	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and can cause permanent damage to the device. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.

[2] Tagore recommends to store parts in moisture barrier bag to preserve solderability.

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Electrical Specifications

Table 5: Electrical Specifications $T_A = +25°C; V_{DD} = +2.7V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency[1]	f	500		2000	MHz
Insertion loss, TX	500 MHz		0.17		dB
$ANT - TX$	915 MHz		0.27		dB
	1200–1310 MHz, IDX01[2]		0.25		dB
Insertion loss, RX	500 MHz		0.75		dB
$ANT - RX$	915 MHz		0.94		dB
	1200–1310 MHz, IDX01[2]		0.71		dB
Isolation	500 MHz		20		dB
$ANT - TX$	915 MHz		15		dB
	1200–1310 MHz, IDX01[2]		27		dB
Isolation	500 MHz		58		dB
$ANT - RX$	915 MHz		52		dB
	1200–1310 MHz, IDX01[2]		47		dB
Return loss	500 MHz		-23		dB
$ANT - TX$ ON[3]	915 MHz		-17		dB
	1200–1310 MHz, IDX01[2]		-30		dB
Return loss	500 MHz		-21		dB
$ANT - RX$ ON[3]	915 MHz		-16		dB
	1200–1310 MHz, IDX01[2]		-20		dB

[1] No external DC blocking capacitors are required on RF pins unless DC voltage is applied on a RF pin. 500 and 915 MHz: EVB without matching components (IDX00).
[2] Matching example with the tuning inductor L_T, see Schematics and Evaluation Board; worst case over the band. Matched values are not guaranteed as they include performance of matching components. These components are beyond control of TagoreTech and therefore given values are indications, not guaranteed values.
[3] Return loss of the ANT port and the active RF port in the given switch state, worst of the two ports.

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Table 6: Electrical Specifications $T_A = +25°C; V_{DD} = +2.7V; 50\Omega$ Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	f	500		2000	MHz
Power and Compression point					
$P_{0.1dB}$ TX[1]	915 MHz, CW (300 W)		>54.8		dBm
$P_{pulse0.1dB}$ TX[1]	915 MHz, 20% duty cycle, 2.0 ms pulse (550 W)		>57.4		dBm
P_{peak} TX[2]	1% duty cycle, LTE / 5G (631 W)	58			dBm
$P_{0.1dB}$ RX[1]	915 MHz, CW (5 W)		37		dBm
$P_{peak0.1dB}$ RX[1]	915 MHz, 1% duty cycle, 10 μs pulse (10 W)		40		dBm
$P_{pulse0.1dB}$ RX[1]	915 MHz, 20% duty cycle, 2.0 ms pulse (8 W)		39		dBm
Switching Time[3]					
t_{ON}	50% ctrl to 90% of RF value, RX / TX		1.1 / 1.4		μs
t_{OFF}	50% ctrl to 10% of RF value, RX / TX		0.4 / 1.6		μs
t_{RISE}	10% to 90% of RF value, RX / TX		0.74 / 0.25		μs
t_{FALL}	90% to 10% of RF value, RX / TX		0.38 / 1.51		μs
Power Supply, DC					
Control voltage	Power Supply V_{DD}	2.6	3.3	5.5	V
	Control pin high[4], V_{ih}	1.0	3.3	5.25	V
	Control pin low, V_{il}	-0.3		0.5	V
Control current	Control pin high, I_{ih}			7.5	μA
	Control pin low, I_{il}		0		μA
Current consumption	I_{DD}, active mode (V_{DD} on)		160	200	μA

[1] $P_{0.1dB}$ is a figure of merit. Please do not exceed Absolute Maximum ratings.
[2] Peak power with 1% duty cycle, for example the envelope peaks of LTE and 5G signals at the TX port: the TS8729N withstands at least 58 dBm (631 W_{peak}).
[3] $C_{VCP} = 100$ nF, internal charge pump.
[4] Control voltage V_{ih} cannot be higher than V_{DD} (to avoid forward biasing of ESD diode)

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Switching time definition

Example of the definition by using 10 W/40 dBm signal. We apply 10W signal to RF port, stabilized with isolator. Isolator is needed as our switch shows to RF port approximately 4Ω impedance. Let's assume that the switch insertion loss is 0.3 dB. Therefore 90% of the RF signal is 39.55 dBm and 10% of the RF signal is 1W/30dBm. We need to take into account 0.3dB insertion loss, therefore numbers are 39.25 dBm and 29.7 dBm respectively. We change the control from low to high and our time reference point is when our control signal exceeds lower threshold value V_{ihlow}. In certain measurements when control signal rise time is significantly shorter than RF output signal, we approximate start of the clock with 50% point of the control signal.

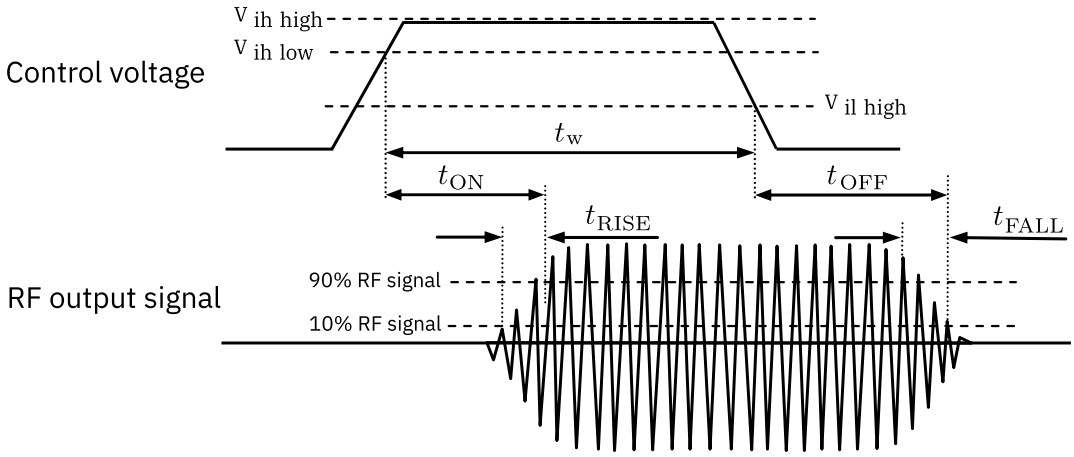

Figure 4: Switching time definition, t_{ON}, t_{OFF}, t_{RISE}, t_{FALL}. Minimum pulse width t_w.

Our component uses integrated charge pump. The switching times of the TS8729N are given with $C_{VCP} = 100$ nF on the V_{CP} pin.

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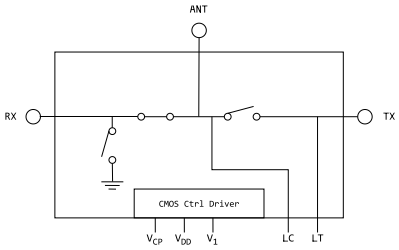
Switch Control table

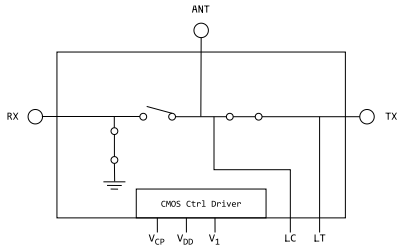
Table 7: Switch Control Table

V_{DD}[1]	V_1	**Switch state**
1	0	$ANT - RX$ ON[2], TX series switch OFF
1	1	$ANT - TX$ ON, RX series switch OFF and RX shunt switch ON
0	0	All switches conducting[3]: TX series, RX series and RX shunt switch ON

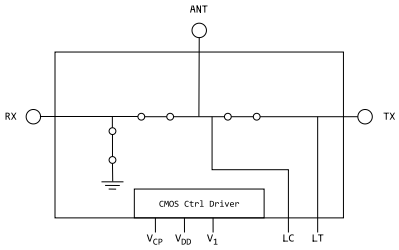
[1] V_{DD} should be applied first before V_1, otherwise may cause damage to the device.
[2] There is an internal pull-down to ground on the V_1 control pin, the state at start-up without any control voltage applied will be $ANT - RX$ ON.
[3] Without supply voltage ($V_{DD} = 0$, $V_1 = 0$) all switches are conducting, see Theory of Operation.



ANT-RX ON ($V_1 = 0$)



ANT-TX ON ($V_1 = 1$)



V_{DD} off, all switches conducting ($V_{DD} = 0$, $V_1 = 0$)

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Theory of Operation

Asymmetrical switch topology

The TS8729N is an asymmetrical SPDT switch optimized for transmit/receive switching. The TX branch between ANT and TX has a series switch only. Without a shunt switch on the TX side, the insertion loss of the TX path is low (0.27 dB at 915 MHz) and the TX path handles high power: 550 W pulse power with 20 % duty cycle and 2.0 ms pulse width, and a peak power of at least 631 W (58 dBm) with 1 % duty cycle, for example with LTE and 5G signals. The RX branch between ANT and RX has a series switch and a shunt switch. In the ANT-TX ON state, the RX series switch is open and the RX shunt switch connects the RX port to ground, which gives high ANT-RX isolation (52 dB at 915 MHz) to protect the receiver. In the ANT-RX ON state, the TX series switch is open; as the TX branch has no shunt switch, the ANT-TX isolation is lower (15 dB at 915 MHz).

Tuning inductor and isolation notch

Pins 17 (LT) and 18 (LC) are connections for an external tuning inductor L_T across the TX series switch. The tuning inductor tunes out the capacitance of the open TX branch: it creates a notch in the ANT-TX isolation curve, and the notch frequency is set by the inductance. Choose L_T for the desired frequency range first, and design the matching networks with the chosen L_T in place. The matching example of this datasheet shows the effect: without L_T the ANT-TX isolation is 13 dB at 1255 MHz; with $L_T = 22$ nH (IDX01) the notch is at 1.3 GHz with 39 dB, and the ANT-TX isolation is at least 27 dB over 1200 to 1310 MHz. When the tuning inductor is not used, pins 17 and 18 are left open.

V_{DD} off state

Without supply voltage ($V_{DD} = 0$, $V_1 = 0$) all switches of the TS8729N are conducting: the TX series switch connects ANT to TX, the RX series switch connects ANT to RX, and the RX shunt switch connects the RX branch to ground. The switch control table shows this state as the third row.

Application Information

TS8729N is offering 550 W pulse power capability with 20 % duty cycle and 2.0 ms pulse width from 500 MHz to 2.0 GHz. Applications include L-band radar, high-power transmit/receive transceivers, tactical radios and LTE and 5G transmit/receive switching; the peak power capability is at least 631 W (58 dBm) with 1 % duty cycle, for example with LTE and 5G signals. In the past, such applications were covered with power hungry and complex PIN diodes, TS8729N significantly reduces design complexity for such RF switching needs. Below 1 GHz the switch works without matching components. For the L-band radar band 1200 to 1310 MHz the datasheet provides a matching example with the tuning inductor (IDX01).

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Schematics and Evaluation Board

S-parameters of all presented EVB configurations (IDX00 and IDX01) can be downloaded from this link: Download TS8729N S-parameters

Table 8: Port definitions in s-parameter files and plots.

PIN name	Port numbers	S-parameters	Function
ANT	1	S11	
RX (RF1)	2	S22	
TX (RF2)	3	S33	
RXON (RF1ON)	12	S21	ANT-RX ON
TXON (RF2ON)	13	S31	ANT-TX ON

Content of s-parameter repository:

```
TS8729N.zip
└── TS8729N
    ├── TS8729N_IDX00 ..... IDX00, no matching components
    │   ├── Readme.txt ..... matching network description
    │   ├── TS8729N_RF1ON_3PORT.s3p ..... S3P file for ANT-RX ON mode
    │   └── TS8729N_RF2ON_3PORT.s3p ..... S3P file for ANT-TX ON mode
    └── TS8729N_IDX_01_1200MHz_1310MHz ..... IDX01, L_T 22 nH, 1200 to 1310 MHz
        ├── Readme.txt ..... matching network description
        ├── TS8729N_RF1ON_3PORT.s3p ..... S3P file for ANT-RX ON mode
        └── TS8729N_RF2ON_3PORT.s3p ..... S3P file for ANT-TX ON mode
```


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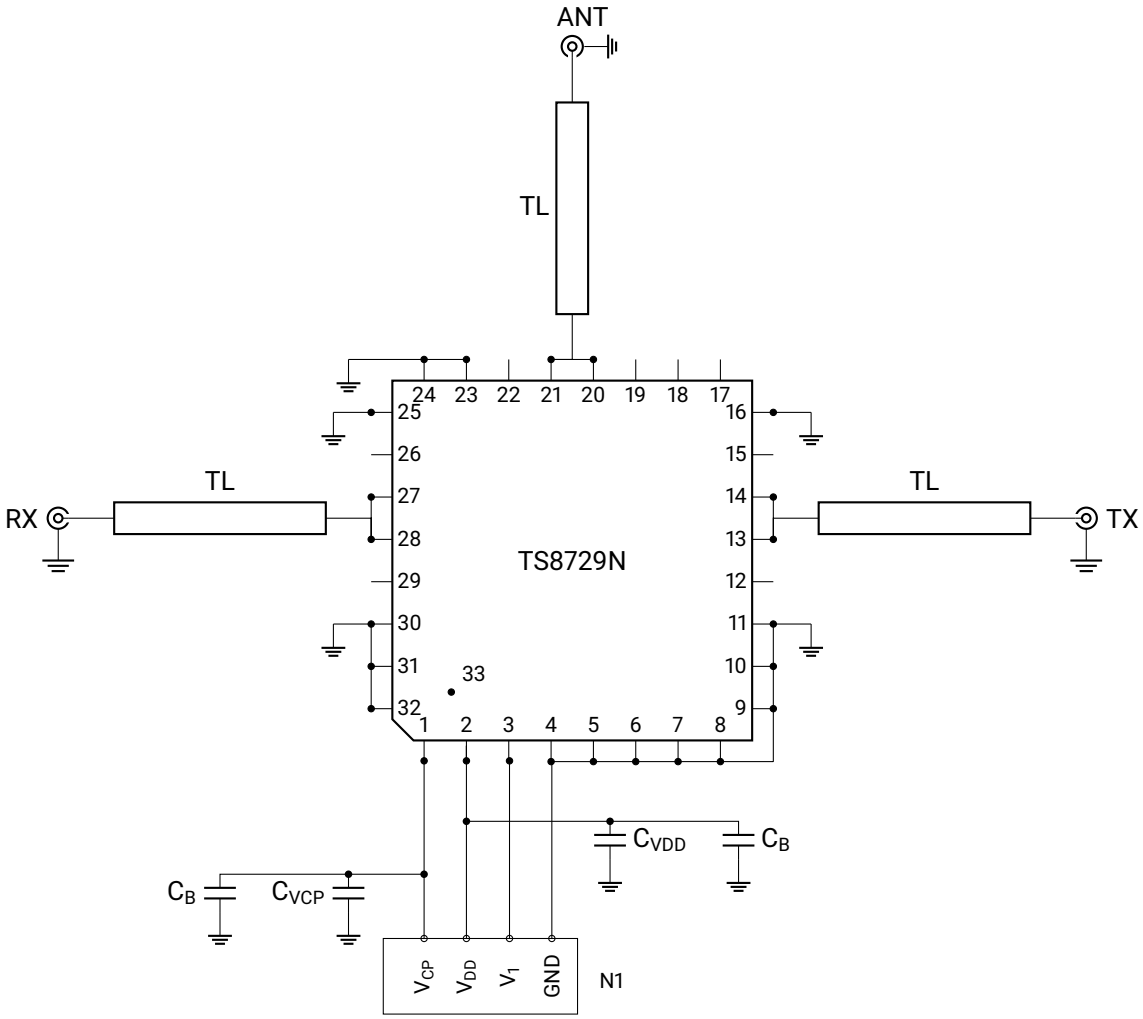
Unmatched EVB (IDX00), up to 1.0 GHz

TS8729N works without matching components below 1.0 GHz. Only two external components are recommended, 100 nF for V_{CP} and 10 nF for V_{DD} lines for supporting charge pump and power supply; the 27 pF capacitors C_B are optional. Pins 17 and 18 are left open. The NC pins next to the RF pins (12, 15, 19, 22, 26 and 29) are not connected on the EVB, not even to ground. Leaving these pins unconnected gives the wider clearance and creepage distance around the RF pins that is needed at high RF voltages. On the EVB, the RX port is the connector RF1 and the TX port is the connector RF2; the plots use the same names.



Schematics of TS8729N EVB without matching components

Table 9: Components used for TS8729N EVB

Reference	Part number / Value	Description	Notes
C_{VDD}	10 nF	Capacitor	GRM155R71H103KA88
C_{VCP}	100 nF	Capacitor	GRM155R61E104KA87D
C_B	27 pF	Capacitor, 200 V	UQCL2A270GAT2A, optional

Pin 33 is the center pad of the device. Multiple plugged through-hole vias should be added on this ground pad and adequate heat sinking should be used.

The purpose of the connection between V_{CP} and connector N1 is to monitor V_{CP}, do not apply an external voltage to V_{CP}.

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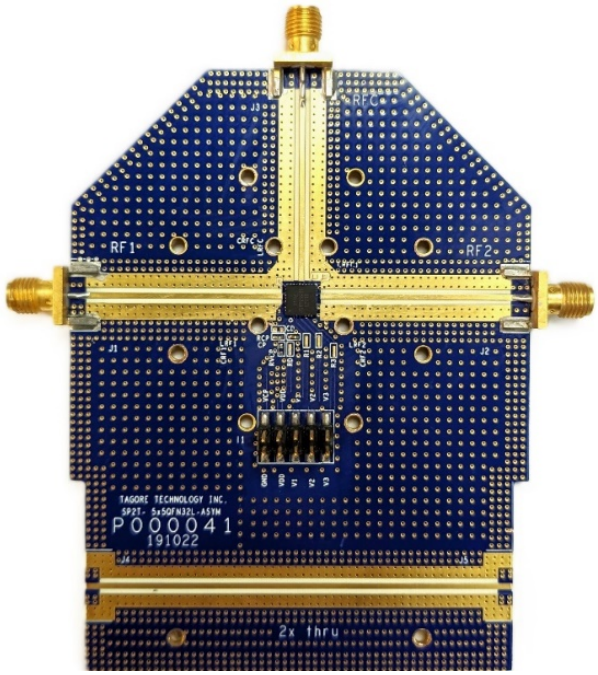

Photo of TS8729N EVB

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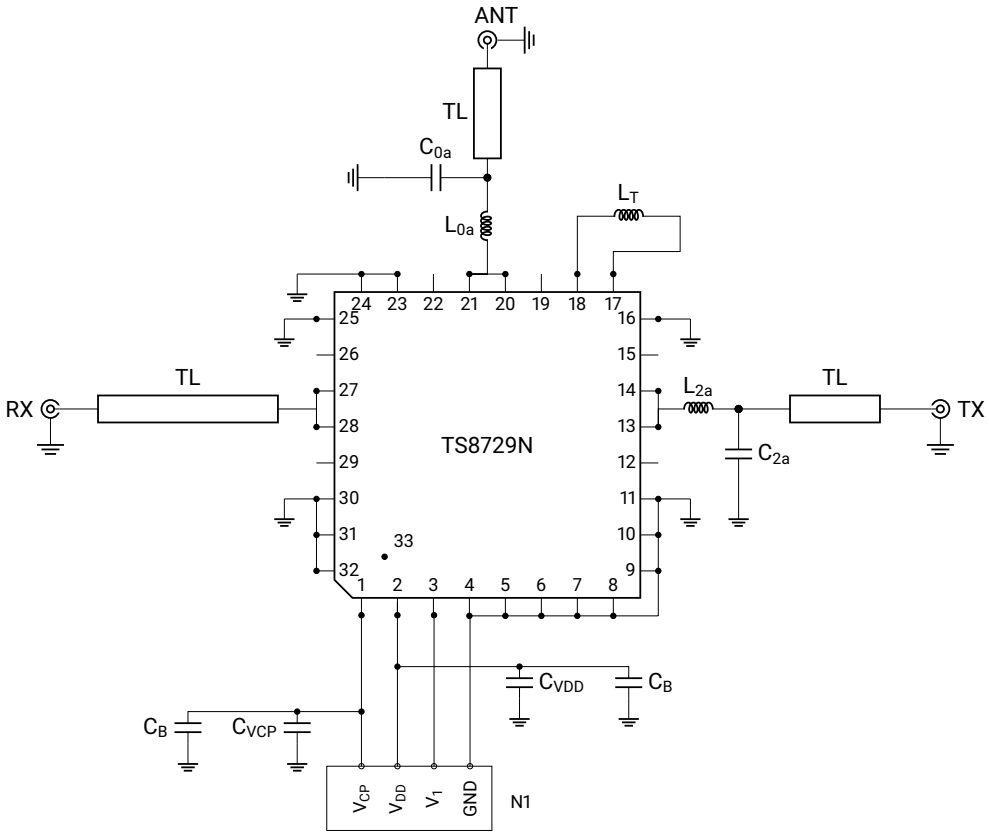
Matching example (IDX01), 1200 to 1310 MHz

The matching example uses the same EVB as the unmatched configuration. The tuning inductor $L_T = 22$ nH between pins 17 and 18 sets the ANT-TX isolation notch to the band; choose L_T first and design the matching networks with L_T in place. At the ANT port and at the TX port, the matching network is a series inductor of 2.8 nH (L_{0a}, L_{2a}, two 5.6 nH inductors in parallel) next to the switch, followed by a shunt capacitor of 0.3 pF (C_{0a}, C_{2a}). The RX port is not matched. Solder the matching components as close as possible to the pins of the switch.



Schematics of TS8729N EVB with the IDX01 matching components

Table 10: Matching components used for IDX01, 1200 to 1310 MHz

Reference	Value	Part number	Description
L_T	22 nH	0402DC-22NX_R_	Ceramic core chip inductor, ±5 %
L_{0a}	2.8 nH[a]	0603DC-5N6X_RW	Ceramic core chip inductor, 5.6 nH, ±5 %, two in parallel
C_{0a}	0.3 pF	0603N0R3BW251	Ceramic capacitor, 250 V, ±0.1 pF
L_{2a}	2.8 nH[a]	0603DC-5N6X_RW	Ceramic core chip inductor, 5.6 nH, ±5 %, two in parallel
C_{2a}	0.3 pF	0603N0R3BW251	Ceramic capacitor, 250 V, ±0.1 pF
C_{VDD}	10 nF	GRM155R71H103KA88	Ceramic capacitor, 50 V
C_{VCP}	100 nF	GRM155R61E104KA87D	Ceramic capacitor, 25 V
C_B	27 pF	UQCL2A270GAT2A	Ceramic capacitor, 200 V, ±2 %, optional

[a] Two 5.6 nH inductors in parallel.

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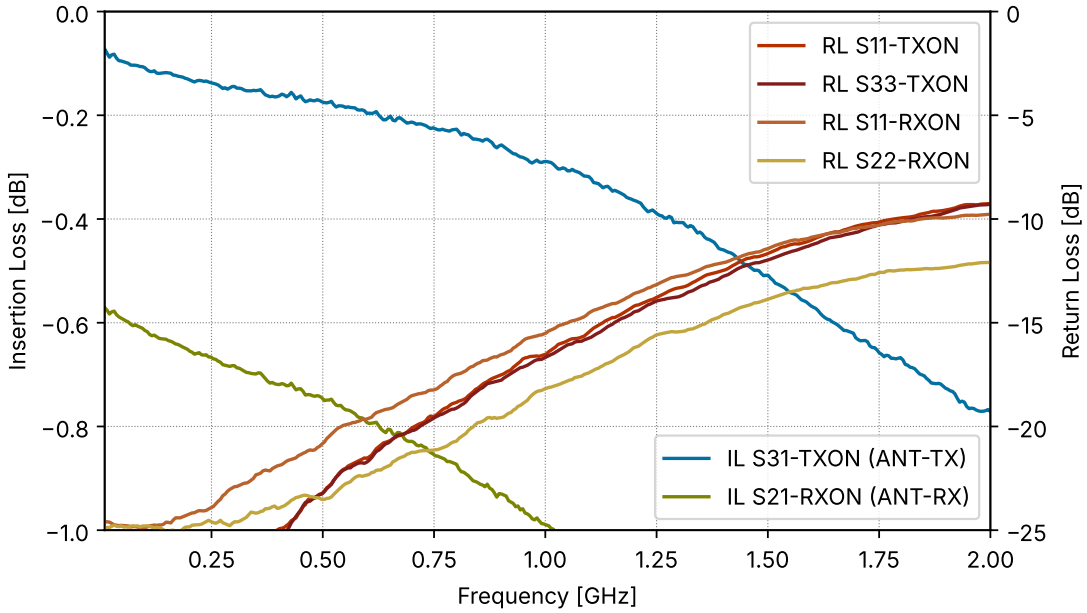
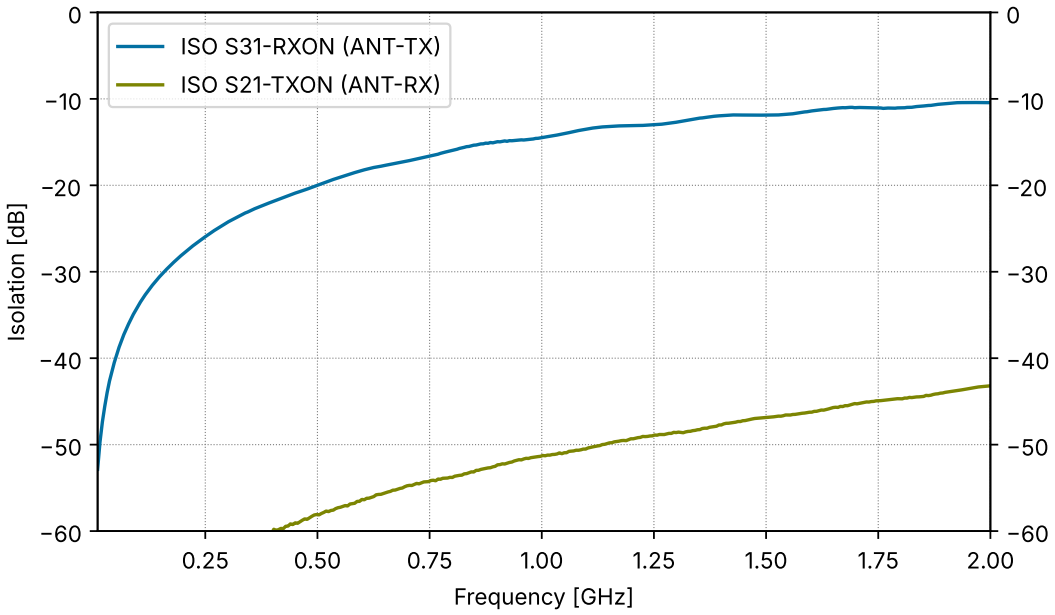
Typical characteristics

Performance up to 2.0 GHz, unmatched (IDX00)

These measurements were obtained using the TS8729N EVB without matching components (IDX00), with CPW losses de-embedded. Without matching components the switch is used up to 1.0 GHz. At 915 MHz the TX insertion loss is 0.27 dB and the RX insertion loss 0.94 dB, the ANT-RX isolation is 52 dB and the ANT-TX isolation 15 dB. The plots extend to 2.0 GHz, the upper end of the operating frequency range; the RX insertion loss exceeds 1 dB above 1.0 GHz.



Insertion loss and return loss.



Isolation of the non-active port, ANT-TX in the ANT-RX ON state and ANT-RX in the ANT-TX ON state.

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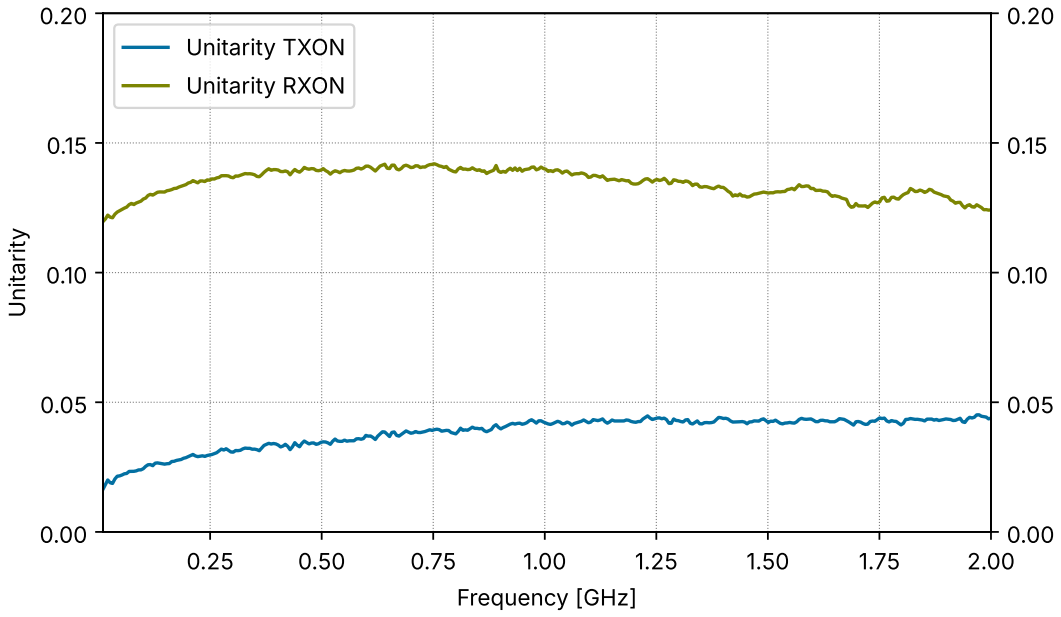
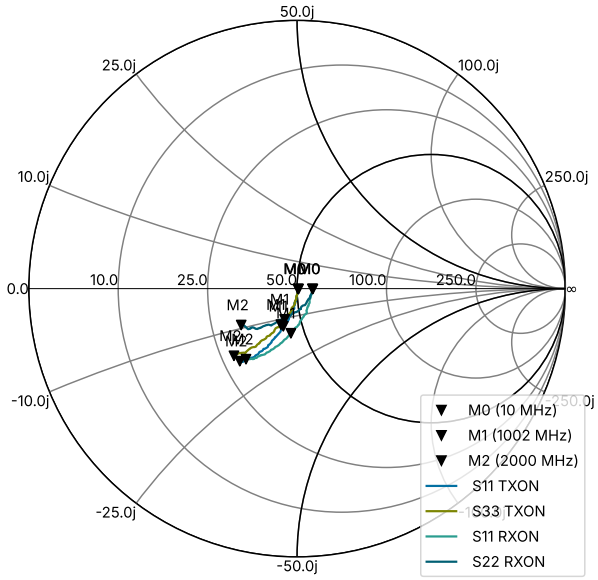
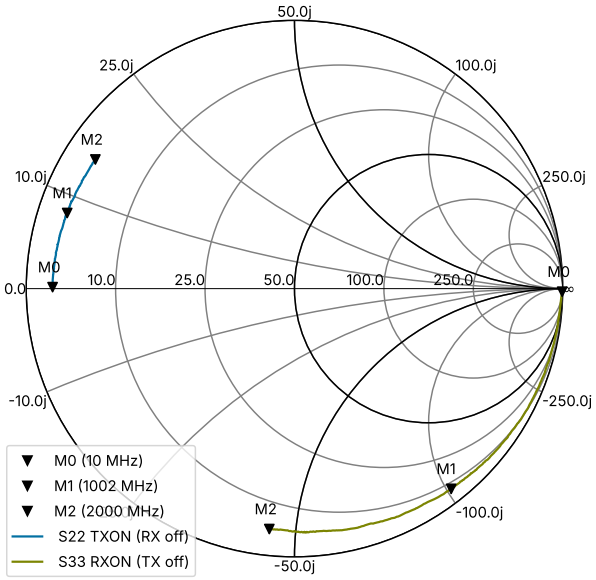


Unitarity, power absorption of the component, $1 - |S_{11}|^2 - |S_{21}|^2 - |S_{31}|^2$.



Matching of the active ports



Termination impedance of the non-active port

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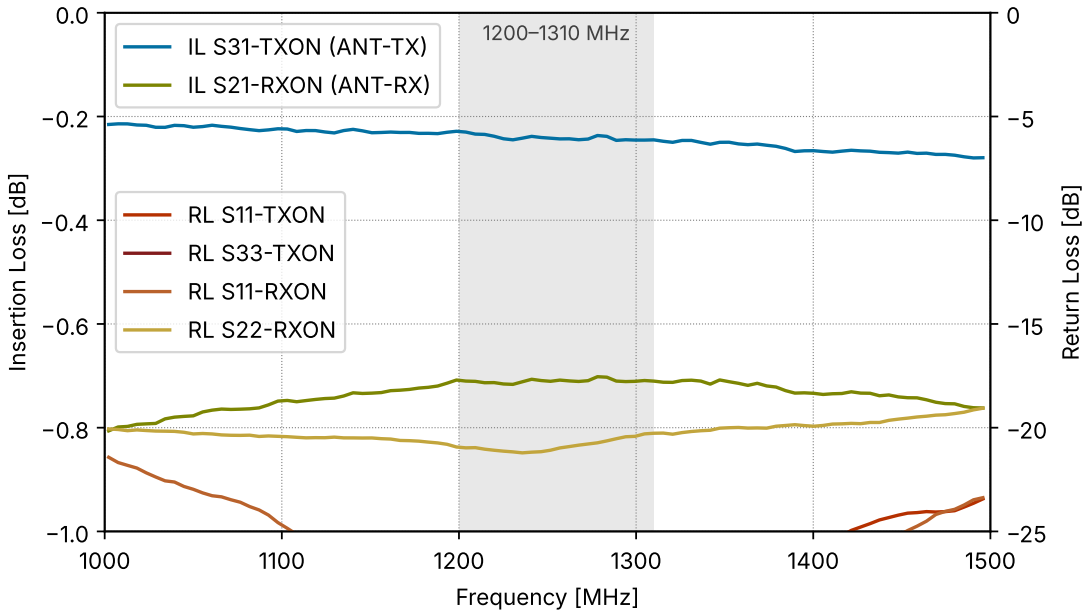
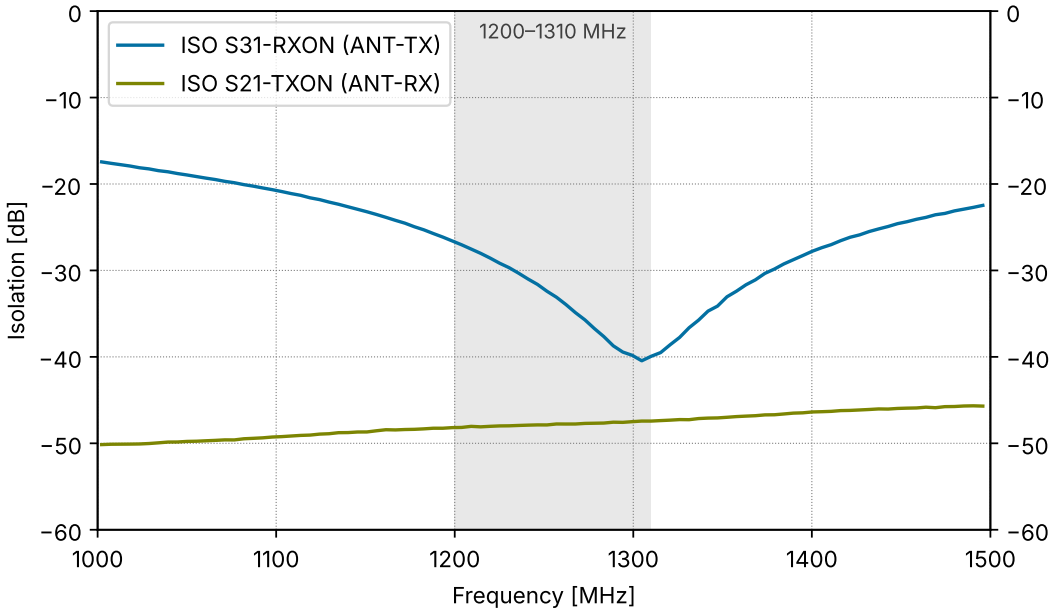
Performance 1200 to 1310 MHz, matched (IDX01)

These measurements were obtained using the TS8729N EVB with the IDX01 matching components ($L_T = 22$ nH, Table 10), including the losses of the matching components. The operating band 1200 to 1310 MHz is shaded grey. Over the band the TX insertion loss is at most 0.25 dB, the RX insertion loss at most 0.71 dB, the ANT-RX isolation at least 47 dB and the ANT-TX isolation at least 27 dB, with the isolation notch at 1.3 GHz.



Insertion loss and return loss, IDX01.



Isolation of the non-active port, ANT-TX in the ANT-RX ON state and ANT-RX in the ANT-TX ON state, IDX01.

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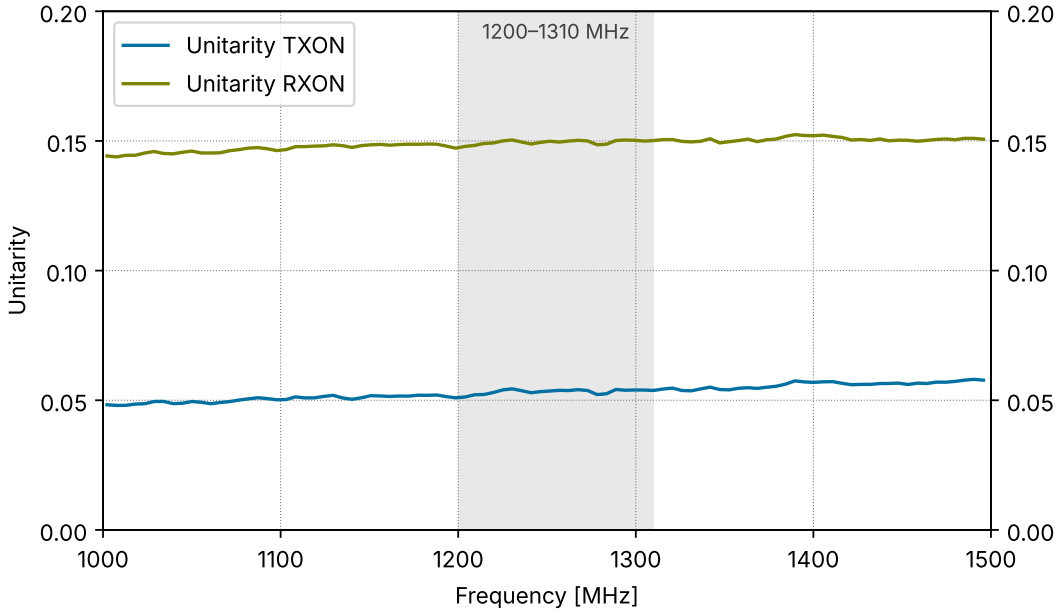
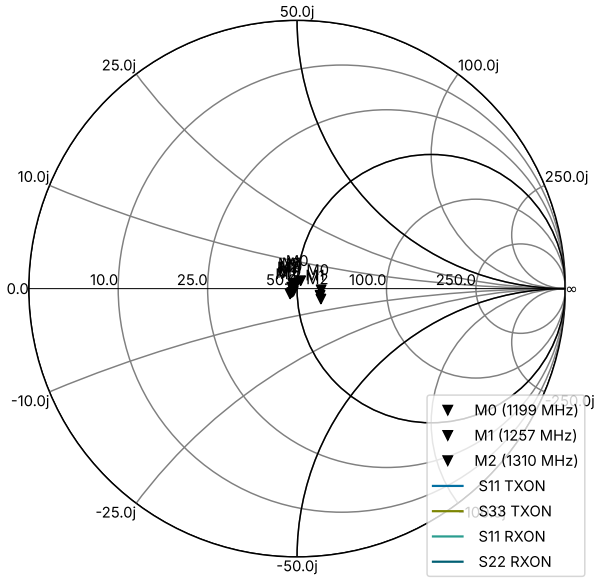
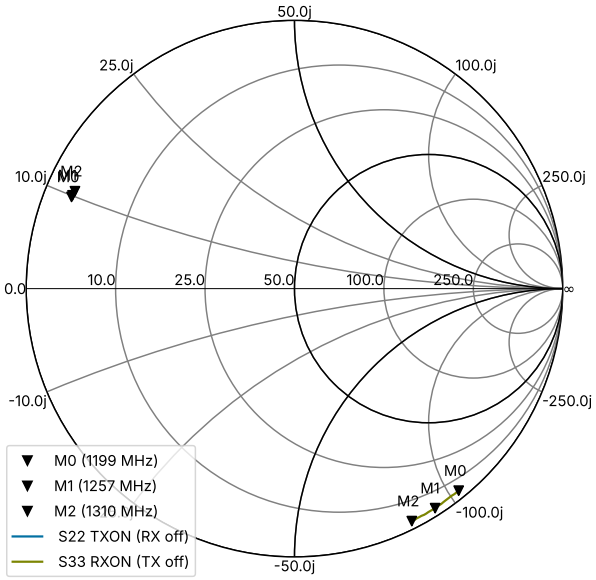


Unitarity, power absorption of the component, $1 - |S_{11}|^2 - |S_{21}|^2 - |S_{31}|^2$, IDX01.



Matching of the active ports



Termination impedance of the non-active port

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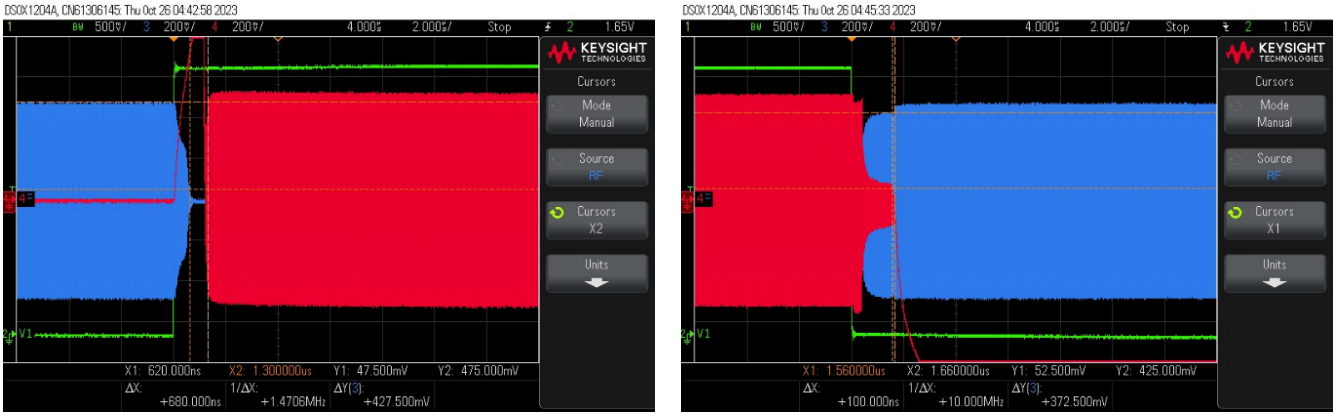
Switching time

Switching time measurements of the TS8729N EVB with $C_{VCP} = 100$ nF. Typical values are given in the Electrical Specifications.



Switching time measurement, control signal and RF envelope.

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Device Package information

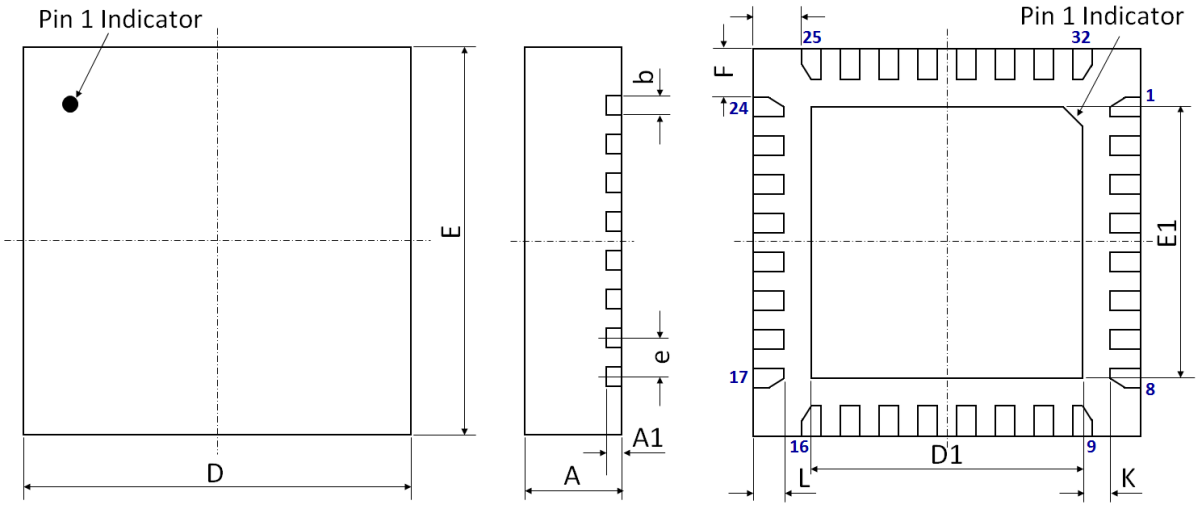

Figure 9: 32-pin QFN 5.0 x 5.0 x 0.75 mm^3 package drawing.

Please refer to application notes TN-001 PCB Design guideline and TN-002 Solder Rework at TagoreTech web page for PCB and soldering guidelines.

Table 11: Device Package Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A	0.75	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	3.10	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	5.00 BSC	±0.05	G	0.625	±0.05
D1	3.10	±0.06	L	0.40	±0.05
e	0.50 BSC	±0.05	K	0.50	±0.05

Lead finish: pure Sn without underlayer; thickness 7.5 μm to 20 μm (typical 10 μm to 12 μm).

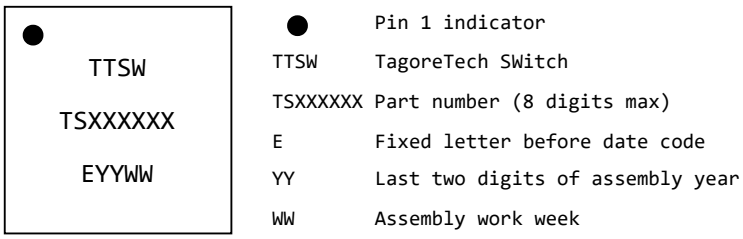

Figure 10: Part marking specification.

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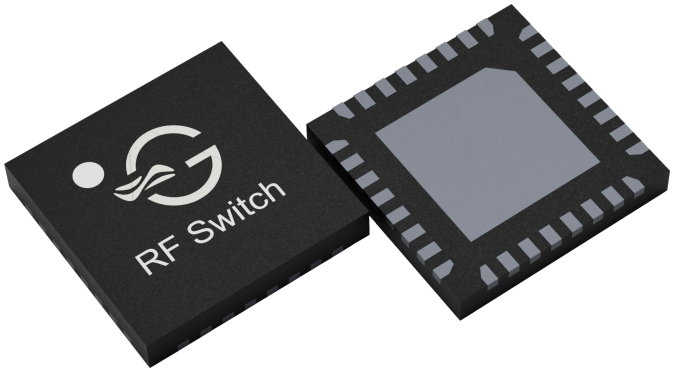

Figure 11: TS8729N, top and bottom side.

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PCB Land Design

Notes:

- 4-layer PCB is recommended.
- Via diameter is recommended to be 0.2 mm to prevent solder wicking inside the vias.
- Thermal vias shall only be placed on the center pad.
- The maximum via number for the center pad is 5(X)×5(Y)=25.

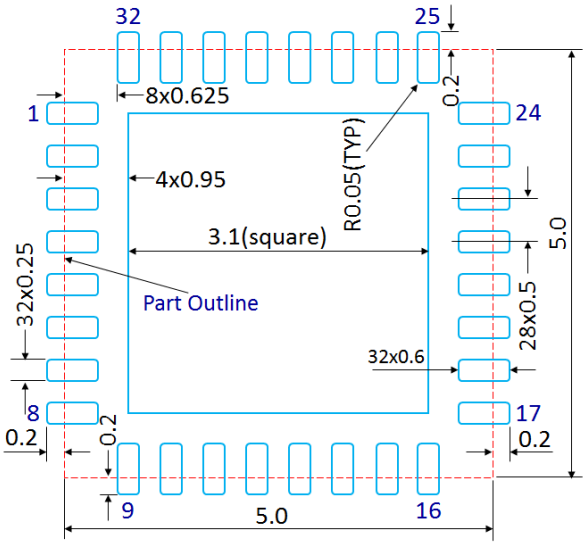

Figure 12: PCB land pattern, dimensions in [mm].



Figure 13: Solder mask pattern, non-solder mask defined (preferred, left) and solder mask defined (right), dimensions in [mm].

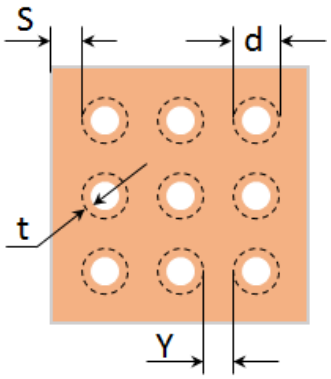

Figure 14: Thermal Via Pattern, Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm.

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PCB Stencil Design

Notes:

- Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- Stencil thickness is recommended to be 125μm.

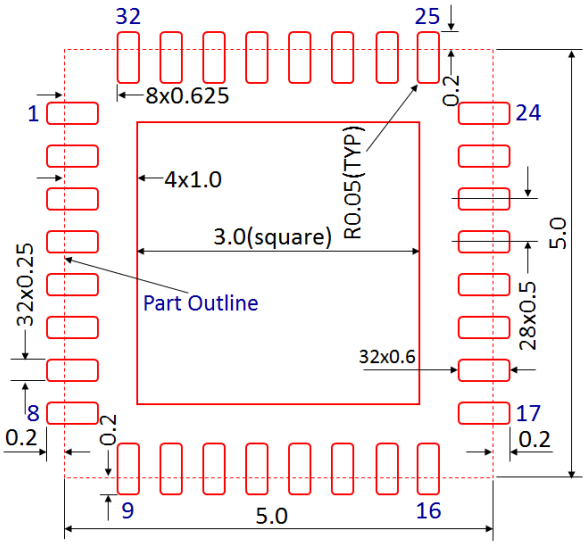

Figure 15: Stencil Openings, dimensions in [mm].

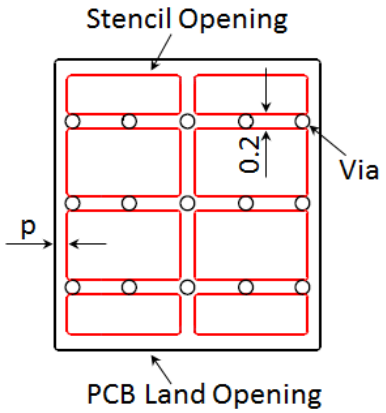

Figure 16: Stencil Openings Shall not Cover Via Areas If Possible, dimensions in [mm].

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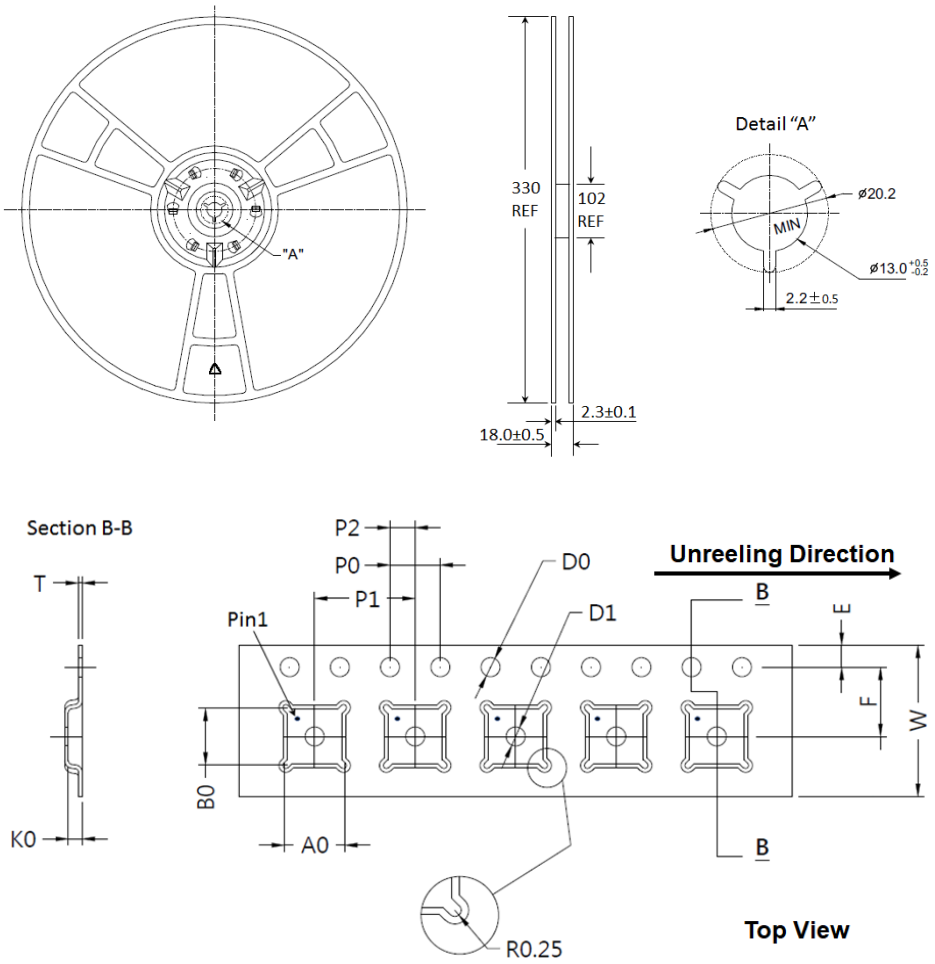
Tape and Reel Information



A0[mm]	B0[mm]	D0[mm]	D1[mm]	E[mm]	F[mm]	K0[mm]	P0[mm]	P1[mm]	P2[mm]	T[mm]	W[mm]
5.35	5.35	1.50	1.50	1.75	5.50	1.10	4.00	8.00	2.00	0.30	12.00

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Glossary

IL	Insertion loss
ISO	Isolation
RL	Return loss
VSWR	Voltage Standing Wave Ratio
ANT	Antenna port, RF common port
TX	Transmit port
RX	Receive port
L_T	External tuning inductor between pins 17 (LT) and 18 (LC)
CPW	Coplanar waveguide
IDX	EVB configuration index of the S-parameter files (IDX00 unmatched, IDX01 matching example)
Unitarity	Describes power absorption of the component, $1 - \lvert S_{11}\rvert^2 - \lvert S_{21}\rvert^2 - \lvert S_{31}\rvert^2$
LTE / 5G	Long Term Evolution / fifth generation mobile network (5G NR)
W_{pulse}	Pulse power: 20 % duty cycle, 2.0 ms pulse width
W_{peak}	Peak power: 1 % duty cycle, for example the envelope peaks of LTE and 5G signals

Changelog

Table 12: Changelog

Date	Revision	Notes
04/23/2026	2.1	Previous datasheet revision (Word).
10/29/2026	3.00	New release in the TagoreTech datasheet format. V_{DD} off state (all switches conducting) added to the switch control table. Asymmetrical topology described: TX branch series switch only, RX branch series and shunt switch. Tuning inductor pins 17 (LT) and 18 (LC) and the isolation notch described. Power ratings: 550 W_{pulse} (20 % duty cycle, 2.0 ms pulse width) and at least 631 W_{peak} (58 dBm, 1 % duty cycle, LTE / 5G). Functional diagram, pin assignment and switch-state drawings in the house style, EVB schematics redrawn. V_{CP} absolute maximum rating -20 V added. Units of the switching times corrected to μs. Typical characteristics of IDX00 and the matching example IDX01 (1200 to 1310 MHz) from the measured S-parameters, matching component table, S-parameter repository; insertion loss, isolation and return loss specifications and front-page values from the same data. Links to application notes TN-001/TN-002, distributor table, QR code link to the latest datasheet, glossary.

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