Single Channel 100 W Receiver Front End 2 GHz to 5 GHz

Discontinued. This datasheet is provided for archiving purposes only. The replacement part is the TagoreTech TSL8028N: TSL8028N product page, TSL8028N datasheet.

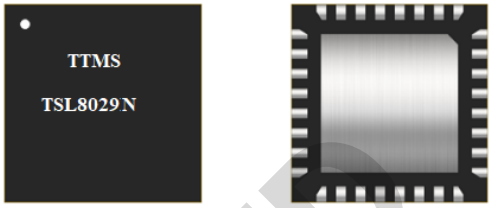

Figure 1: TSL8029N in 5 x 5 x 0.85 mm 32-lead QFN package.

Features

- Integrated single-channel RF front end: 2-stage LNA and GaN SPDT switch
- On-chip bias and matching, single-supply operation
- Gain @ 3.6 GHz: 33 dB (high gain mode), 14.5 dB (low gain mode)
- NF @ 3.6 GHz: 1.4 dB (high gain mode), 1.3 dB (low gain mode)
- OP1dB @ 3.6 GHz: 22 dBm (high gain mode), 12 dBm (low gain mode)
- Operating frequency: 2 GHz – 5 GHz
- Insertion loss @ 3600 MHz: 0.5 dB (TX mode)
- Switch isolation @ 3.6 GHz: 18 dB (RX HG mode)
- RX isolation @ 3.6 GHz: 53 dB (PD $=$ BP $=$ 0 V), 42 dB (PD $=$ BP $=$ 5 V), 38 dB (PD $=$ 0 V, BP $=$ 5 V), 45 dB (PD $=$ 5 V, BP $=$ 0 V)
- High power handling at $T_{CASE} = 105\,°C$, full lifetime: LTE average power (8 dB PAR) 50 dBm
- High OIP3 (high gain mode): 31 dBm typical
- Current at 5 V: 90 mA (high gain), 45 mA (low gain), 4 mA (power-down) typical
- Positive logic control
- 5 mm $\times$ 5 mm $\times$ 0.85 mm, 32-lead QFN

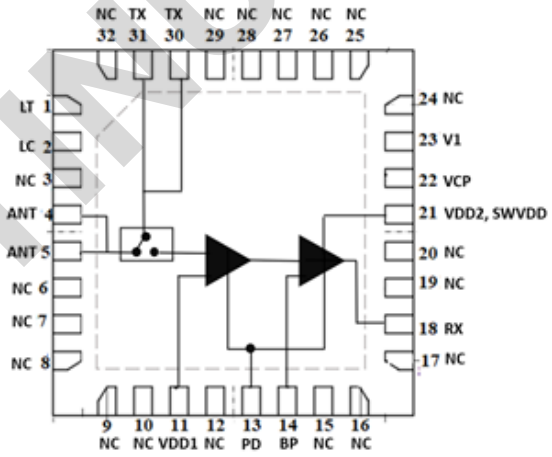

Figure 2: TSL8029N function block diagram (top view).

Applications

- 4G/5G infrastructure radios, macro base station
- Small cells and cellular repeaters
- Phase array radar
- SDARS

RoHS/REACH/Halogen free

Replacement part: TagoreTech **TSL8028N** (TSL8028N datasheet).

Scan for the TSL8028N datasheet

DISCONTINUED

General Description

The TSL8029N is a single-channel, integrated RF front-end multichip module designed for different applications. The device operates from 2 GHz to 5 GHz. The TSL8029N is configured with a cascading two-stage GaAs LNA and a GaN based SPDT switch.

In high gain mode, the cascaded two-stage LNA and switch offer a low noise figure of 1.3 dB and a high gain of 33 dB at 3.6 GHz with an output third-order intercept point (OIP3) of 33 dBm (typical). In low gain mode, one stage of the two-stage LNA is in bypass, providing 14.5 dB of gain at a lower current of 50 mA. In power-down mode, the LNAs are turned off and the device draws 4 mA.

In transmit operation, when the RF input is connected to the termination pin (TX), the switch provides a low insertion loss of 0.5 dB at 3.6 GHz and handles a long-term evolution (LTE) average power (8 dB peak to average ratio (PAR)) of 50 dBm for full lifetime operation.

The device comes in an RoHS compliant, compact 5 mm × 5 mm, 32-lead QFN.

The TSL8029N is discontinued. The replacement part is the TSL8028N (TSL8028N datasheet).

Contents

Features 1
Applications 1
General Description 2
Ordering information 3
Pin Assignment 4
Absolute Maximum Ratings 5
Recommended DC Operating Conditions 6
Control Truth Tables 7
RF Electrical Specifications 8
Switching Speed 13
Typical characteristics 14
Receive operation, low gain mode . . . 14
Receive operation, high gain mode . . . 16
Transmit mode . . . 18
Evaluation Boards 19
2300 to 2700 MHz EVB A . . . 19
3300 to 4200 MHz EVB B (high gain only) . . . 20
3300 to 4200 MHz EVB C . . . 21
3300 to 3800 MHz EVB D (high gain only) . . . 22
2900 to 3300 MHz EVB E . . . 23
Test Procedure 24
Biasing sequence . . . 24
Test set-up . . . 24
Device Package information 26
PCB Land Design 27
PCB Stencil Design 29
Tape and Reel Information 30
Glossary 31
Changelog . . . 31
Legal Information 32
Published by . . . 32
Legal Disclaimer . . . 32
Sales Contact . . . 32
Replacement part: TSL8028N . . . 32
TSL8029N Product Information . . . 32
TagoreTech Inc. Product Brochure and datasheets . . . 32

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Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TSL8029N	32-pin 5x5x0.85 mm QFN	Base part number, discontinued
TSL8029NMTRPBF[1]	330 mm (13”) reel, 3 000 pcs	Full reel
TSL8029N-EVB-A	Tuned evaluation board	2300 to 2700 MHz
TSL8029N-EVB-B	Tuned evaluation board	3300 to 4200 MHz (high gain only)
TSL8029N-EVB-C	Tuned evaluation board	3300 to 4200 MHz
TSL8029N-EVB-D	Tuned evaluation board	3300 to 3800 MHz (high gain only)
TSL8029N-EVB-E	Tuned evaluation board	2900 to 3300 MHz

[1] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.
The TSL8029N is discontinued. The replacement part is the TSL8028N.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	330 mm (13”)	18 mm

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Pin Assignment

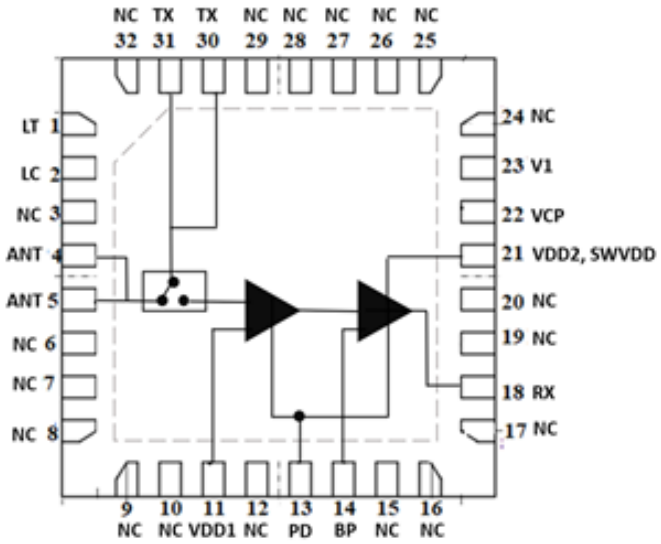

Figure 3: TSL8029N pin assignment and function block diagram [top view]

Table 3: Pin Definition

Pin Number	Pin Name	Description
1, 2	L_T, L_C	Tuning inductor
3, 6–10, 12, 15–17, 19, 20, 24–29, 32	NC	Not internally connected. It is recommended to connect NC to the RF ground of the PCB.
4, 5	ANT	RF input. The ANT pin is ac-coupled to 0 V and matched to 50 Ω. Matching and a dc blocking capacitor are not required.
11	V_{DD1}	V_{DD1} supplied through an external choke inductor
13	PD	Power-down all stages of the LNA[2]
14	BP	Bypass second stage LNA[2]
18	RX	Receiver output. The RX pin is the receiver path for the channel. The RX pin is ac matched to 50 Ω. No matching component is required. A dc blocking capacitor is required.
21	V_{DD2}/SWV_{DD}	V_{DD2}/SWV_{DD} supply voltage through an external choke inductor to the LNA; also the supply voltage of the switch.
22	V_{CP}	Internal charge pump voltage output. Connect a 1 nF capacitor to GND on this pin to improve the switching time.
23	V_1	Control voltage for the switch.
30, 31	TX	Termination output. The TX pin is the transmitter path. The TX pin is ac-coupled to 0 V and matched to 50 Ω. No matching and dc blocking capacitor is required.
Package base[1]	Paddle/Slug	DC and RF ground. Also provides thermal relief. Multiple vias are recommended.

[1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heatsink required.
[2] The source datasheet gives the PD and BP descriptions the other way round; corrected according to the pin names, the function block diagram and the truth tables.

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Supply voltage, V_{DD1}, V_{DD2}, SWV_{DD}	V_{DD}	+5.5	V
RF input power, transmit input power (LTE peak, 8 dB PAR)	RF_{IN}	58	dBm
RF input power, receive input power (LTE peak, 8 dB PAR)	RF_{IN}	25	dBm
Digital control input voltage, V_1, BP and PD		2.6 to 5.5	V
Digital control input current, V_1, BP and PD		0.2	mA
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +105	°C
Maximum Junction Temperature	T_j	170	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	15.0	°C/W
Soldering Temperature	T_{solder}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 – $<$1000	V
Charged Device Model (CDM)	Level C	$\geq$1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

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Recommended DC Operating Conditions

Table 5: Recommended Operating Conditions, $T_A = +25$°C unless otherwise specified

Parameter	Symbol / Condition	Min	Typ	Max	Unit
Drain voltages	V_{DD1}		+5.0		V
	V_{DD2}		+5.0		V
Drain bias currents	I_{DQ1}, set by external drain feed		50		mA
	I_{DQ2}, set by external drain feed		90		mA
Switch supply	SWV_{DD}		+5		V
Switch control voltages	V_1, BP and PD	-0.3		+5.5	V
RF input power in TX mode at ANT	$V_1 = 5$ V, PD $= 5$ V, BP $= 0$ V, 8 dB PAR LTE, full lifetime average		50		dBm
	$V_1 = 5$ V, PD $= 0$ V, BP $= 0$ V, 8 dB PAR LTE, full lifetime average			TBD	dBm
	$V_1 = 5$ V, PD $= 0$ V, BP $= 5$ V, 8 dB PAR LTE, full lifetime			TBD	dBm
Digital inputs V_1, PD	Low, V_{IL}	-0.3		0.5	V
	High, V_{IH}	2.6		V_{DD}	V
Digital inputs BP	Low, V_{IL}	0		0.5	V
	High, V_{IH}	2.6		V_{DD}	V
Digital input currents	$V_1 = 5$ V			$<$7.5	μA
	PD $= 5$ V			200	μA
	BP $= 5$ V			100	μA
Switch control maximum current				7.5	μA
Operating temperature range	T_{op}	-40	+25	+105	°C

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Control Truth Tables

Table 6: Truth Table: Switch Control

	Signal path select	
V_1 **(switch control)**	**Transmit operation**	**Receive operation**
Low	Off	On
High	On	Off

Table 7: Truth Table: Receive Operation

Receive operation	**PD**	**BP**	**Signal path**
High gain mode	Low	Low	ANT to RX
Low gain mode	Low	High	ANT to RX
Power-down mode (LNA in high gain setting)	High	Low	ANT to RX
Power-down mode (LNA in low gain setting)	High	High	ANT to RX

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RF Electrical Specifications

V_{DD1}, $V_{DD2}/SWV_{DD} = 5$ V, BP $= 0$ V / 5 V and PD $= 0$ V, $T_{CASE} = +25$°C, 50 Ω system, unless otherwise noted.

Table 8: RF Electrical Specifications, 2300 to 2700 MHz EVB A

Parameter	Test Condition	Min	Typ	Max	Unit
Operating frequency		2.3		2.7	GHz
Gain	LNAs on, bypass off (high gain)		34		dB
	LNA1 on, bypass on (low gain)		14 – 14.5		dB
Noise figure (de-embedded)	LNAs on, bypass off (high gain)		1		dB
	LNA1 on, bypass on (low gain)		1		dB
Noise figure (SMA to SMA)	LNAs on, bypass off (high gain)		1.2		dB
	LNA1 on, bypass on (low gain)		1.2		dB
Input return loss	LNAs on, bypass off (high gain)		< -9.3		dB
	LNA1 on, bypass on (low gain)		< -8.5		dB
Output return loss	LNAs on, bypass off (high gain)		< -8.4		dB
	LNA1 on, bypass on (low gain)		< -4		dB
OP1dB	LNAs on, bypass off (high gain)		20 – 21		dBm
	LNA1 on, bypass on (low gain)		14 – 16		dBm
OIP3	LNAs on, bypass off (high gain), 0 dBm per tone, tone spacing 1 MHz		29.5 – 31.5		dBm
	LNA1 on, bypass on (low gain), -2 dBm per tone, tone spacing 1 MHz		23 – 30		dBm
Current, I_d	LNAs on, bypass off (high gain)		93		mA
	LNA1 on, bypass on (low gain)		55		mA
	PD mode on (both LNAs off)		4		mA
Insertion loss (SMA to SMA)	Transmit operation		0.7 – 0.9		dB
Insertion loss (de-embedded)	Transmit operation		0.5 – 0.7		dB
Switch isolation in RX mode	PD $=$ BP $= V_1 = 0$ V		> 25		dB

Typical values given as a range over the operating frequency range of the EVB, as in the source datasheet.

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Table 9: RF Electrical Specifications, 3300 to 4200 MHz EVB B (high gain only)

Parameter	Test Condition	Min	Typ	Max	Unit
Operating frequency		3.3		4.2	GHz
Gain	LNAs on, bypass off (high gain)		29.5 – 32.4		dB
Noise figure (de-embedded)	LNAs on, bypass off (high gain)		1.3 – 1.4		dB
Noise figure (SMA to SMA)	LNAs on, bypass off (high gain)		1.5 – 1.6		dB
Input return loss	LNAs on, bypass off (high gain)		< -10.5		dB
Output return loss	LNAs on, bypass off (high gain)		< -7.5		dB
OP1dB	LNAs on, bypass off (high gain)		19 – 21		dBm
OIP3	LNAs on, bypass off (high gain), 0 dBm per tone, tone spacing 1 MHz		31 – 37		dBm
Current, I_d	LNAs on, bypass off (high gain)		93		mA
	PD mode on (both LNAs off)		4 – 5		mA
Insertion loss (SMA to SMA)	Transmit operation at 3.6 GHz		0.7		dB
Insertion loss (de-embedded)	Transmit operation at 3.6 GHz		0.5		dB
Switch isolation in RX mode	PD = BP = $V_1 = 0$ V		> 19.7		dB

Typical values given as a range over the operating frequency range of the EVB, as in the source datasheet.

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Table 10: RF Electrical Specifications, 3300 to 4200 MHz EVB C

Parameter	Test Condition	Min	Typ	Max	Unit
Operating frequency		3.3		4.2	GHz
Gain	LNAs on, bypass off (high gain)		29.5 – 32.4		dB
	LNA1 on, bypass on (low gain)		12.5 – 14		dB
Noise figure (de-embedded)	LNAs on, bypass off (high gain)		1.4		dB
	LNA1 on, bypass on (low gain)		1.3		dB
Noise figure (SMA to SMA)	LNAs on, bypass off (high gain)		1.6		dB
	LNA1 on, bypass on (low gain)		1.5		dB
Input return loss	LNAs on, bypass off (high gain)		< -10.5		dB
	LNA1 on, bypass on (low gain)		< -13		dB
Output return loss	LNAs on, bypass off (high gain)		< -7		dB
	LNA1 on, bypass on (low gain)		< -7		dB
OP1dB	LNAs on, bypass off (high gain)		19 – 21		dBm
	LNA1 on, bypass on (low gain)		11 – 12.5		dBm
OIP3	LNAs on, bypass off (high gain), 0 dBm per tone, tone spacing 1 MHz		31 – 37		dBm
	LNA1 on, bypass on (low gain), -2 dBm per tone, tone spacing 1 MHz		20 – 22		dBm
Current, I_d	LNAs on, bypass off (high gain)		93		mA
	LNA1 on, bypass on (low gain)		55		mA
	PD mode on (both LNAs off)		4		mA
Insertion loss (SMA to SMA)	Transmit operation		0.7 – 0.75		dB
Insertion loss (de-embedded)	Transmit operation		0.4 – 0.5		dB
Switch isolation in RX mode	PD $=$ BP $=$ $V_1 = 0$ V		> 18.5		dB

Typical values given as a range over the operating frequency range of the EVB, as in the source datasheet.

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Table 11: RF Electrical Specifications, 3300 to 3800 MHz EVB D (high gain only)

Parameter	Test Condition	Min	Typ	Max	Unit
Operating frequency		3.3		3.8	GHz
Gain	LNAs on, bypass off (high gain)		30.5 – 31		dB
Noise figure (de-embedded)	LNAs on, bypass off (high gain)		1.2 – 1.3		dB
Noise figure (SMA to SMA)	LNAs on, bypass off (high gain)		1.4 – 1.5		dB
Input return loss	LNAs on, bypass off (high gain)		< -17		dB
Output return loss	LNAs on, bypass off (high gain)		< -16		dB
OP1dB	LNAs on, bypass off (high gain)		20 – 22		dBm
OIP3	LNAs on, bypass off (high gain), -2 dBm per tone, tone spacing 1 MHz		29 – 34		dBm
Current, I_d	LNAs on, bypass off (high gain)		108		mA
	PD mode on (both LNAs off)		4 – 5		mA
Insertion loss (SMA to SMA)	Transmit operation at 3.6 GHz		0.7		dB
Insertion loss (de-embedded)	Transmit operation at 3.6 GHz		0.4		dB
Switch isolation in RX mode	PD $=$ BP $=$ $V_1 = 0$ V		> 25.7		dB

Typical values given as a range over the operating frequency range of the EVB, as in the source datasheet.

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Table 12: RF Electrical Specifications, 2900 to 3300 MHz EVB E

Parameter	Test Condition	Min	Typ	Max	Unit
Operating frequency		2.9		3.3	GHz
Gain	LNAs on, bypass off (high gain)		31 – 33		dB
	LNA1 on, bypass on (low gain)		13.5 – 13.8		dB
Noise figure (de-embedded)	LNAs on, bypass off (high gain)		1.2 – 1.3		dB
	LNA1 on, bypass on (low gain)		1.2 – 1.3		dB
Noise figure (SMA to SMA)	LNAs on, bypass off (high gain)		1.4 – 1.5		dB
	LNA1 on, bypass on (low gain)		1.4 – 1.5		dB
Input return loss	LNAs on, bypass off (high gain)		< -10.5		dB
	LNA1 on, bypass on (low gain)		< -11.2		dB
Output return loss	LNAs on, bypass off (high gain)		< -10.2		dB
	LNA1 on, bypass on (low gain)		< -6		dB
OP1dB	LNAs on, bypass off (high gain)		20 – 21		dBm
	LNA1 on, bypass on (low gain)		12 – 13.5		dBm
OIP3	LNAs on, bypass off (high gain), 0 dBm per tone, tone spacing 1 MHz		30.5 – 32		dBm
	LNA1 on, bypass on (low gain), -1 dBm per tone, tone spacing 1 MHz		22 – 30		dBm
Current, I_d	LNAs on, bypass off (high gain)		90		mA
	LNA1 on, bypass on (low gain)		50		mA
	PD mode on (both LNAs off)		4		mA
Insertion loss (SMA to SMA)	Transmit operation at 3.6 GHz		0.7 – 0.8		dB
Insertion loss (de-embedded)	Transmit operation at 3.6 GHz		0.4 – 0.5		dB
Switch isolation in RX mode	PD = BP = $V_1 = 0$ V		> 19		dB

Typical values given as a range over the operating frequency range of the EVB, as in the source datasheet.

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Switching Speed

Table 13: TX Switching Speed

Parameter	Test condition	Switching time	Mode
t_{ON}, t_{OFF}	50 % control voltage (V_1) to 90 %, 10 % of RX output in receive operation (TX to RX)	1200 ns	TX/RX mode
t_{ON}, t_{OFF}	50 % control voltage (V_1) to 90 %, 10 % of TX output in transmit operation (RX to TX)	1200 ns	TX/RX mode

Table 14: RX Switching Speed

Pin toggled	State	Switching time	Mode	DC condition
BP	LG to HG	200 ns	RX mode	$V_{DD2}/SWV_{DD} = 5$ V, $V_1 = 5$ V, $V_{DD1} = 5$ V, PD $= 0$ V
	HG to LG	450 ns	RX mode	$V_{DD2}/SWV_{DD} = 5$ V, $V_1 = 5$ V, $V_{DD1} = 5$ V, PD $= 0$ V
PD	Low gain, on to off	360 ns	RX-LG mode	$V_{DD2}/SWV_{DD} = 5$ V, $V_1 = 5$ V, $V_{DD1} = 5$ V, PD $= 0$ V and BP $= 0$ V
	Low gain, off to on	450 ns	RX-LG mode	$V_{DD2}/SWV_{DD} = 5$ V, $V_1 = 5$ V, $V_{DD1} = 5$ V, PD $= 0$ V and BP $= 0$ V
PD	High gain, on to off	360 ns	RX-HG mode	$V_{DD2}/SWV_{DD} = 5$ V, $V_1 = 5$ V, $V_{DD1} = 5$ V, PD $= 0$ V and BP $= 5$ V
	High gain, off to on	720 ns	RX-HG mode	$V_{DD2}/SWV_{DD} = 5$ V, $V_1 = 5$ V, $V_{DD1} = 5$ V, PD $= 0$ V and BP $= 5$ V

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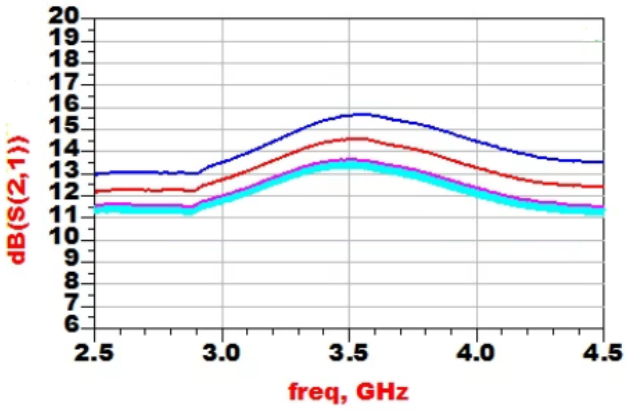
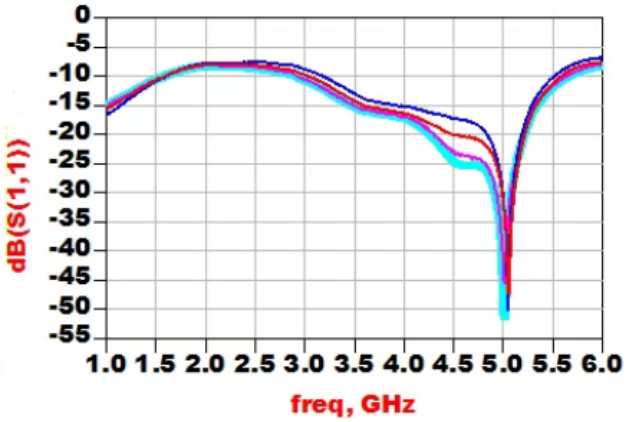
Typical characteristics

Measured on the 3.3 to 4.2 GHz tuned EVB C at $+25$°C, -40°C, $+85$°C and $+105$°C.

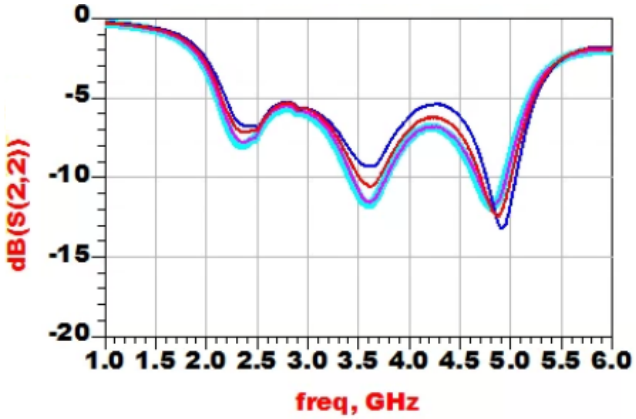
Receive operation, low gain mode



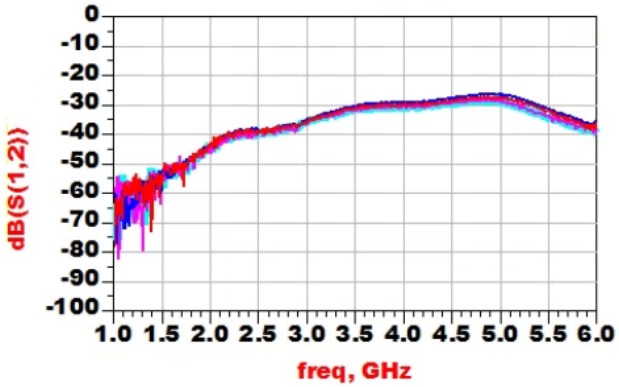
S21 (gain) vs frequency



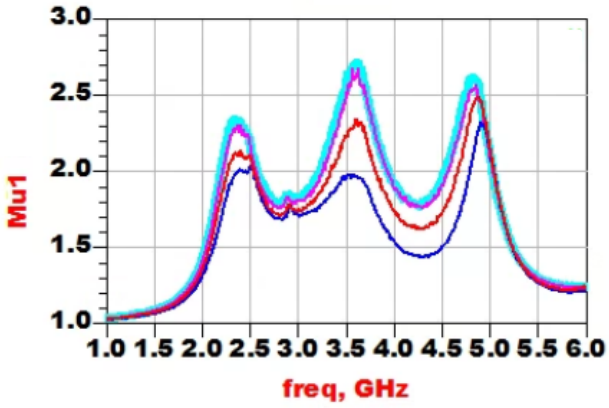
S11 vs frequency



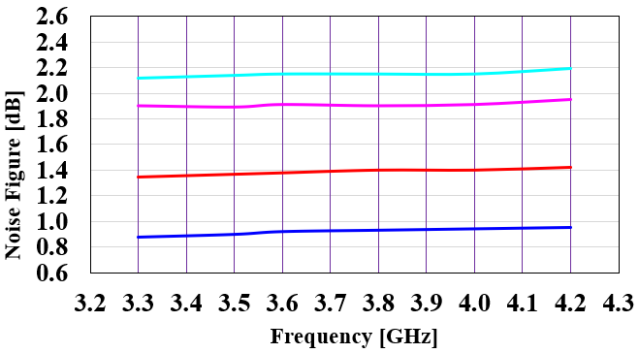
S22 vs frequency



S12 vs frequency



Stability (Mu1) vs frequency



NF vs frequency, SMA to SMA

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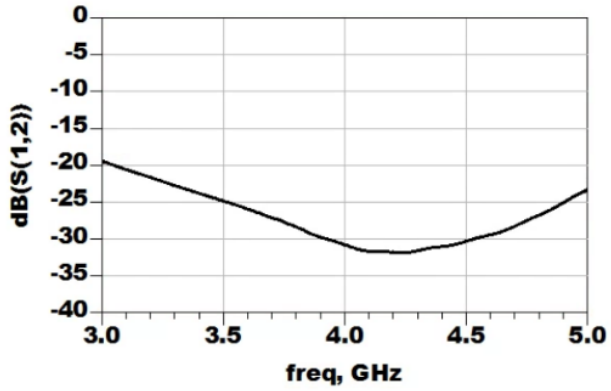
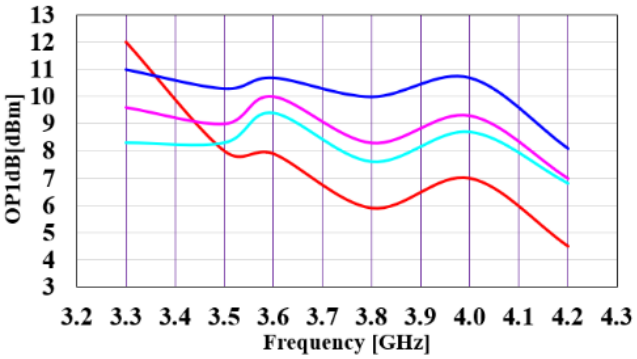
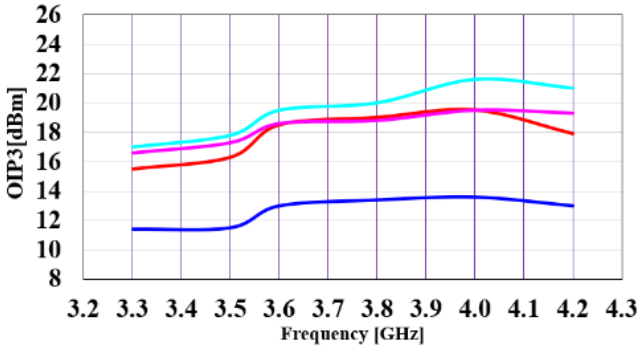


ANT – TX isolation vs frequency, BP $= 5$ V and PD $= 0$ V



OP1dB vs frequency



OIP3 vs frequency

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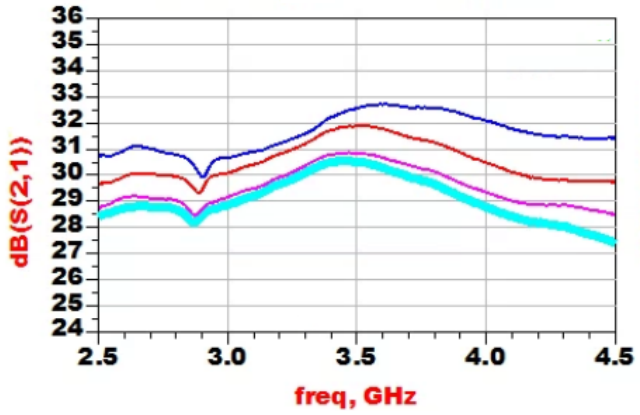
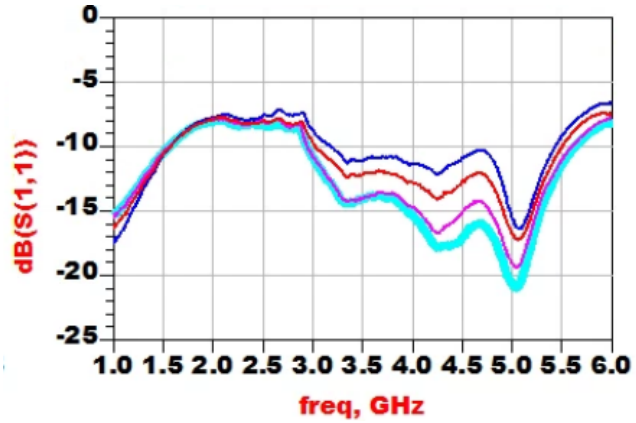
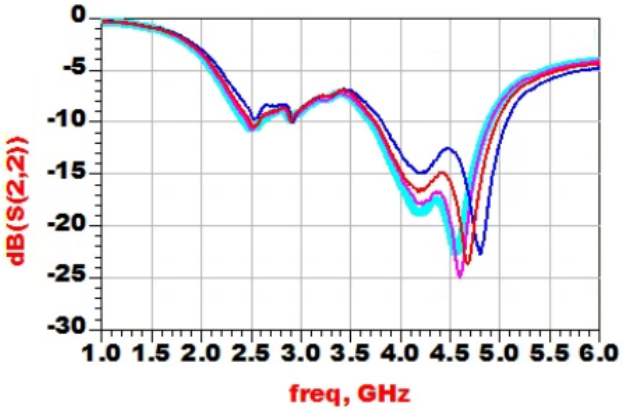
Receive operation, high gain mode



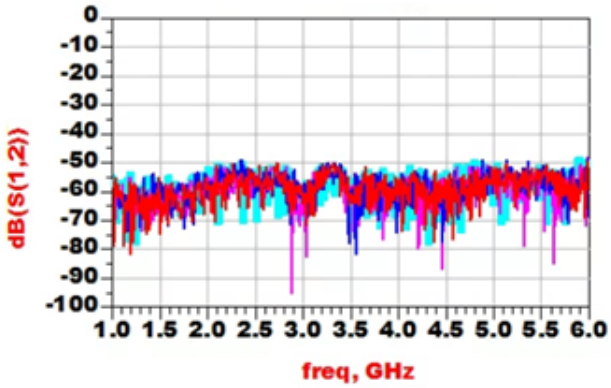
S21 (gain) vs frequency



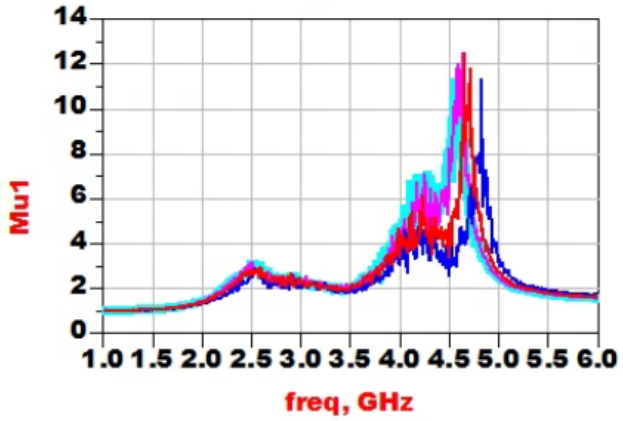
S11 vs frequency



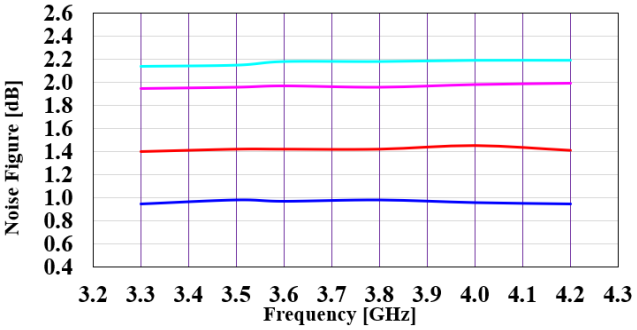
S22 vs frequency



S12 vs frequency



Stability (Mu1) vs frequency, 10 MHz to 8.5 GHz



NF vs frequency, SMA to SMA

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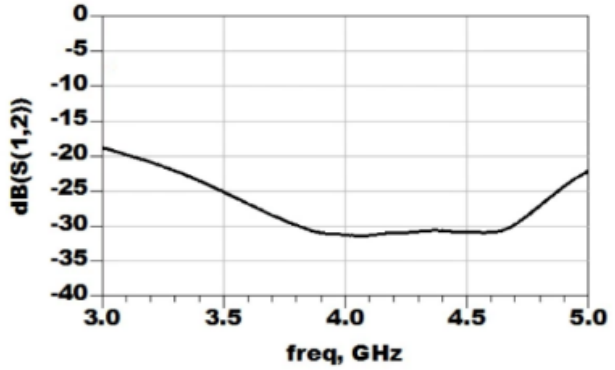
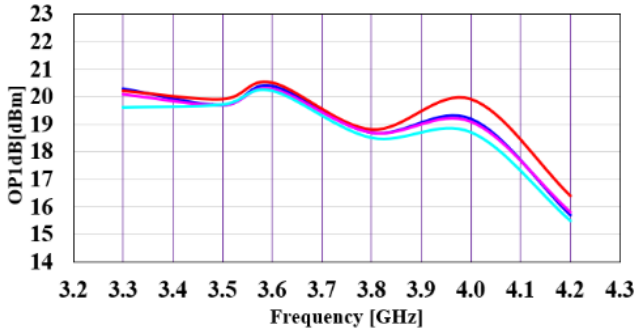
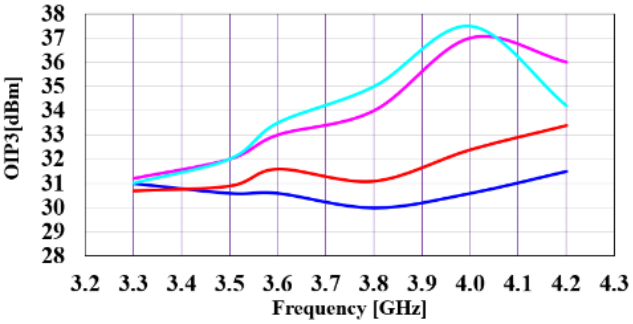


ANT – TX isolation vs frequency, BP $= 0$ V and PD $= 5$ V



OP1dB vs frequency



OIP3 vs frequency

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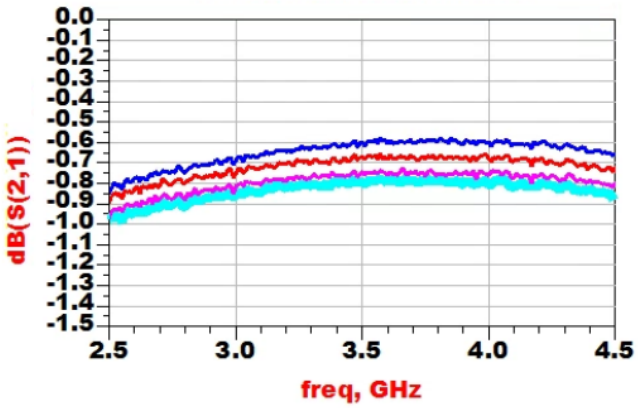
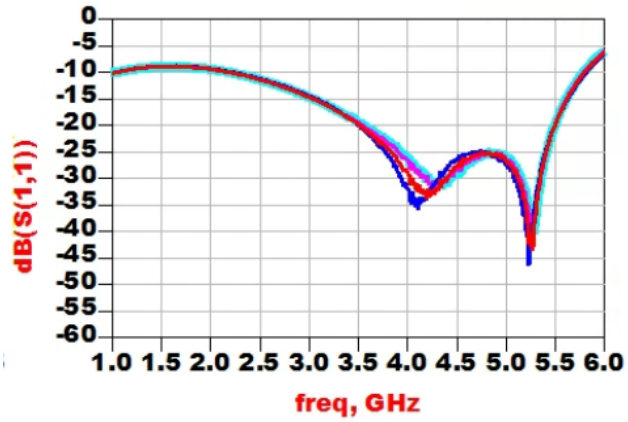
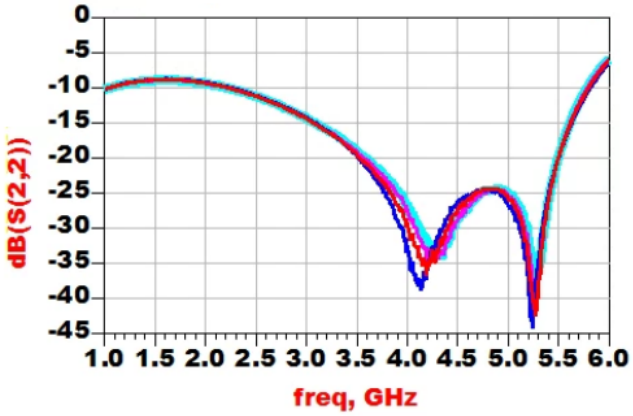
Transmit mode



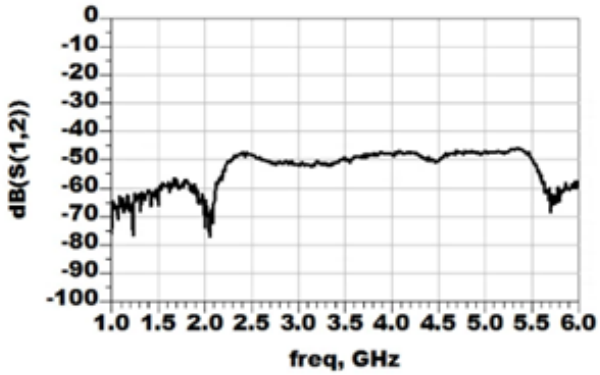
S21 (insertion loss) vs frequency



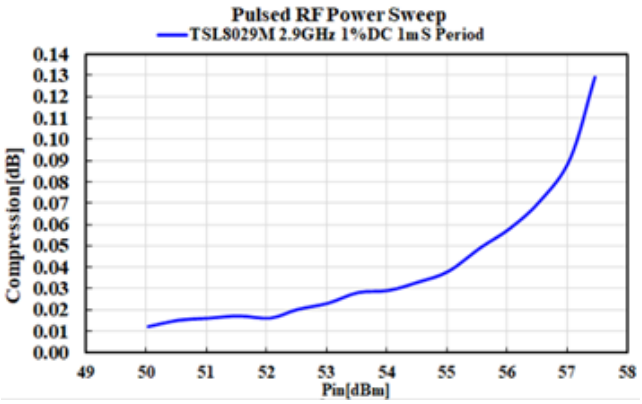
S11 vs frequency



S22 vs frequency



ANT – RX isolation vs frequency, PD $= 5$ V and BP $= 0$ V



Compression vs peak power (2.9 GHz, 1 % duty cycle, 1 ms period)

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Evaluation Boards

2300 to 2700 MHz EVB A

RF electrical specifications in Table 8.

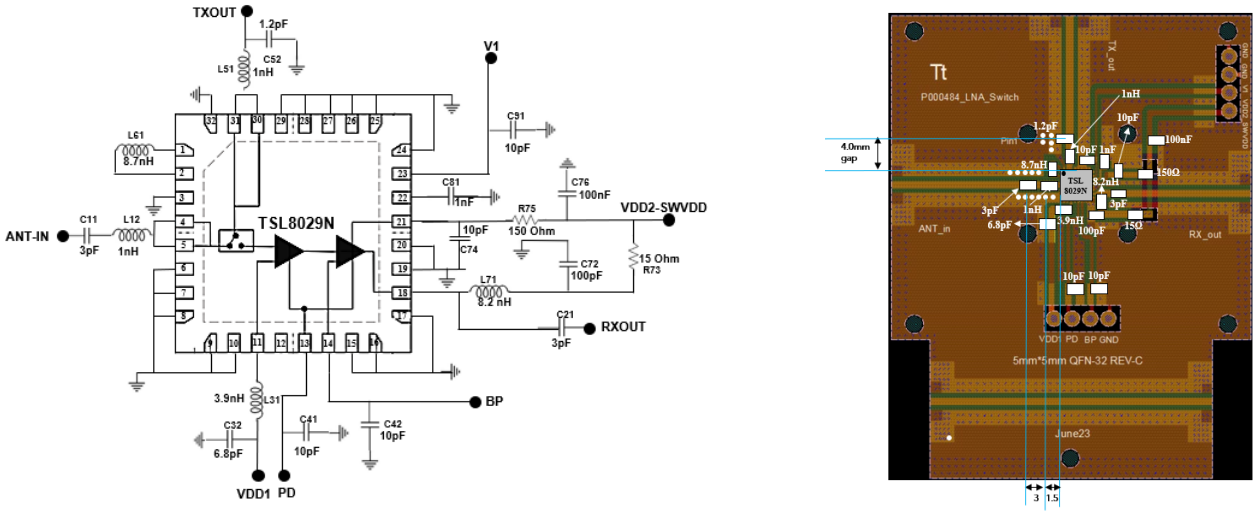

Figure 9: Schematic and layout of the 2300 to 2700 MHz EVB A

Table 15: BOM of the 2300 to 2700 MHz EVB A

Component ID	Value	Manufacturer	Recommended part number	Qty
C11, C21	3 pF	Murata	600S3R0BT250XT	2
L12, L51	1 nH	Coilcraft	0402DC-1N0XJRW	2
L31	3.9 nH	Coilcraft	0402DC-3N9XGRW	1
C32	6.8 pF	Murata	GJM1555C1H6R8BB01D	1
C41, C42, C74, C91	10 pF	Murata	GJM1555C1H100JB01D	4
C52	1.2 pF	Murata	600S1R2BT250XT	1
L61	8.7 nH	Coilcraft	0402HP-8N7XGRW	1
L71	8.2 nH	Coilcraft	0402HP-8N2XGRW	1
C72	100 pF	AVX	04025A101JAT4A	1
R73	15 Ω	Panasonic	ERJ-H2RD15R0X	1
R75	150 Ω	Panasonic	ERJ-2RHD1500X	1
C76	100 nF	TDK	C1005X7R1H104K050BE	1
C81	1 nF	Murata	04025C102JAT2A	1
PCB	Rogers RO4350B, 20 mil, 1 oz copper			1

Note: Series cap on ANT and TX ports should have 250 V voltage ratings to handle 100 W power. The heatsink needs to be added at the bottom of this board for proper power spreading.

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3300 to 4200 MHz EVB B (high gain only)

RF electrical specifications in Table 9.

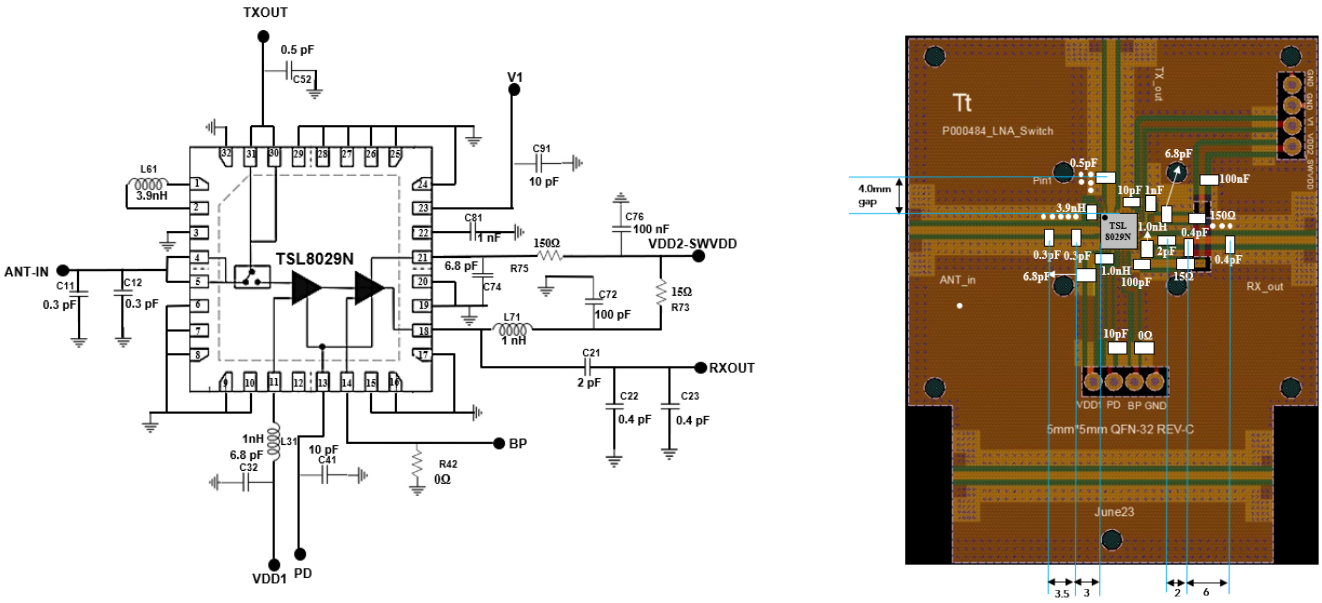

Figure 10: Schematic and layout of the 3300 to 4200 MHz EVB B (high gain only)

Table 16: BOM of the 3300 to 4200 MHz EVB B (high gain only)

Component ID	Value	Manufacturer	Recommended part number	Qty
C11, C12	0.3 pF	Murata	600S0R3BT250XT	2
C21	2 pF	Murata	GJM1555C1H2R0BB01D	1
C22, C23	0.4 pF	Murata	GJM1555C1HR40BB01J	2
L31, L71	1 nH	Coilcraft	0402DC-1N0XJRW	2
C32, C74	6.8 pF	Murata	GJM1555C1H6R8BB01D	2
C41, C91	10 pF	Murata	GJM1555C1H100JB01D	2
R42	0 Ω	Panasonic	ERJ-2GE0R00X	1
C52	0.5 pF	Murata	600S0R5BT250XT	1
L61	3.9 nH	Coilcraft	0402DC-3N9XGRW	1
C72	100 pF	AVX	04025A101JAT4A	1
R73	15 Ω	Panasonic	ERJ-H2RD15R0X	1
R75	150 Ω	Panasonic	ERJ-2RHD1500X	1
C76	100 nF	TDK	C1005X7R1H104K050BE	1
C81	1 nF	Murata	04025C102JAT2A	1
PCB	Rogers RO4350B, 20 mil, 1 oz copper			1

Note: Series cap on ANT and TX ports should have 250 V voltage ratings to handle 100 W power. The heatsink needs to be added at the bottom of this board for proper power spreading.

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3300 to 4200 MHz EVB C

RF electrical specifications in Table 10.

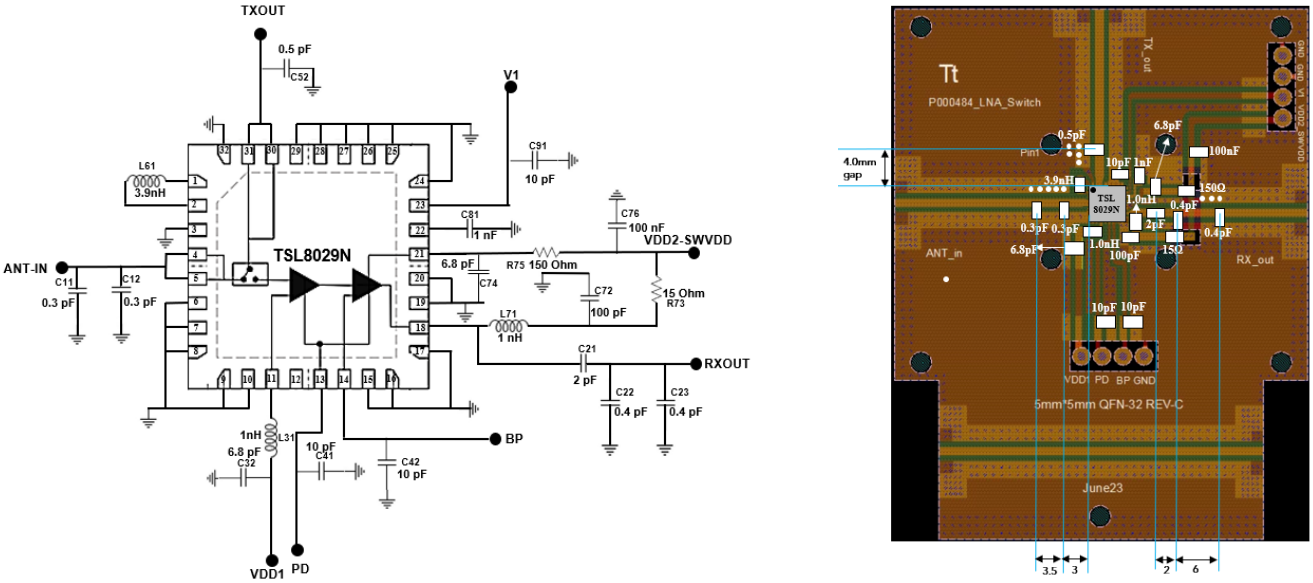

Figure 11: Schematic and layout of the 3300 to 4200 MHz EVB C

Table 17: BOM of the 3300 to 4200 MHz EVB C

Component ID	Value	Manufacturer	Recommended part number	Qty
C11, C12	0.3 pF	Murata	600S0R3BT250XT	2
C21	2 pF	Murata	GJM1555C1H2R0BB01D	1
C22, C23	0.4 pF	Murata	GJM1555C1HR40BB01J	2
L31, L71	1 nH	Coilcraft	0402DC-1N0XJRW	2
C32, C74	6.8 pF	Murata	GJM1555C1H6R8BB01D	2
C41, C42, C91	10 pF	Murata	GJM1555C1H100JB01D	3
C52	0.5 pF	Murata	600S0R5BT250XT	1
L61	3.9 nH	Coilcraft	0402DC-3N9XGRW	1
C72	100 pF	AVX	04025A101JAT4A	1
R73	15 Ω	Panasonic	ERJ-H2RD15R0X	1
R75	150 Ω	Panasonic	ERJ-2RHD1500X	1
C76	100 nF	TDK	C1005X7R1H104K050BE	1
C81	1 nF	Murata	04025C102JAT2A	1
PCB	Rogers RO4350B, 20 mil, 1 oz copper			1

Note: Series cap on ANT and TX ports should have 250 V voltage ratings to handle 100 W power. The heatsink needs to be added at the bottom of this board for proper power spreading.

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3300 to 3800 MHz EVB D (high gain only)

RF electrical specifications in Table 11.

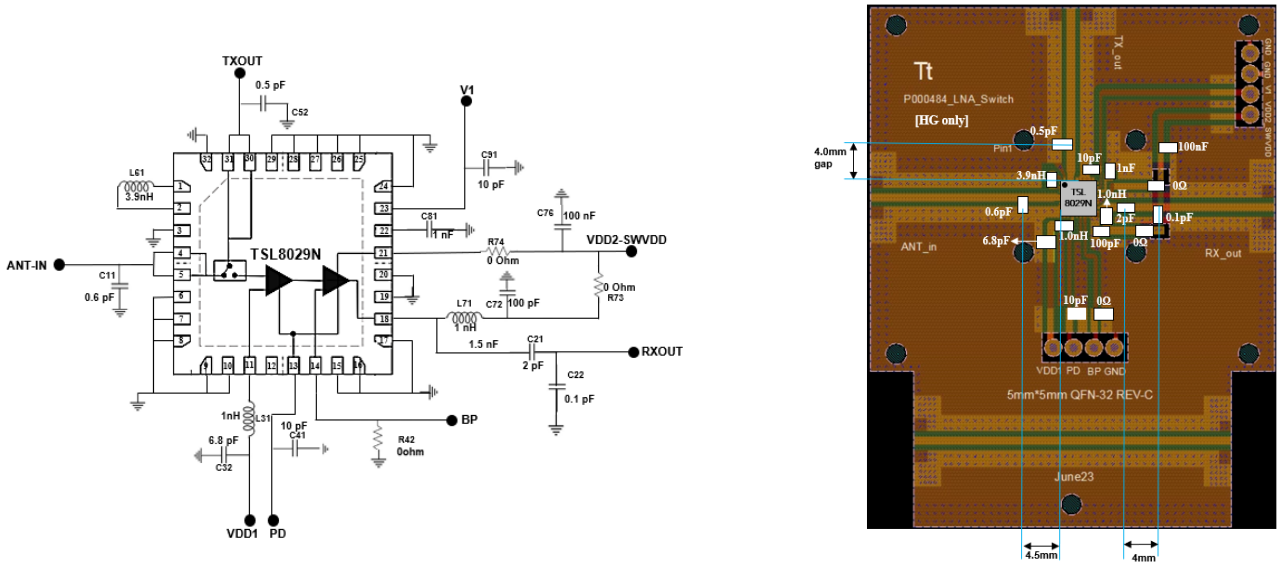

Figure 12: Schematic and layout of the 3300 to 3800 MHz EVB D (high gain only)

Table 18: BOM of the 3300 to 3800 MHz EVB D (high gain only)

Component ID	Value	Manufacturer	Recommended part number	Qty
C11	0.6 pF	Murata	600S0R6BT250XT	1
C21	2 pF	Murata	GJM1555C1H2R0BB01D	1
C22	0.1 pF	Murata	GJM1555C1HR10BB01J	1
L31, L71	1 nH	Coilcraft	0402DC-1N0XJRW	2
C32	6.8 pF	Murata	GJM1555C1H6R8BB01D	1
C41, C91	10 pF	Murata	GJM1555C1H100JB01D	2
R42, R73, R74	0 Ω	Panasonic	ERJ-2GE0R00X	3
C52	0.5 pF	Murata	600S0R5BT250XT	1
L61	3.9 nH	Coilcraft	0402DC-3N9XGRW	1
C72	100 pF	AVX	04025A101JAT4A	1
C76	100 nF	TDK	C1005X7R1H104K050BE	1
C81	1 nF	Murata	04025C102JAT2A	1
PCB	Rogers RO4350B, 20 mil, 1 oz copper			1

Note: Series cap on ANT and TX ports should have 250 V voltage ratings to handle 100 W power. The heatsink needs to be added at the bottom of this board for proper power spreading.

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2900 to 3300 MHz EVB E

RF electrical specifications in Table 12.

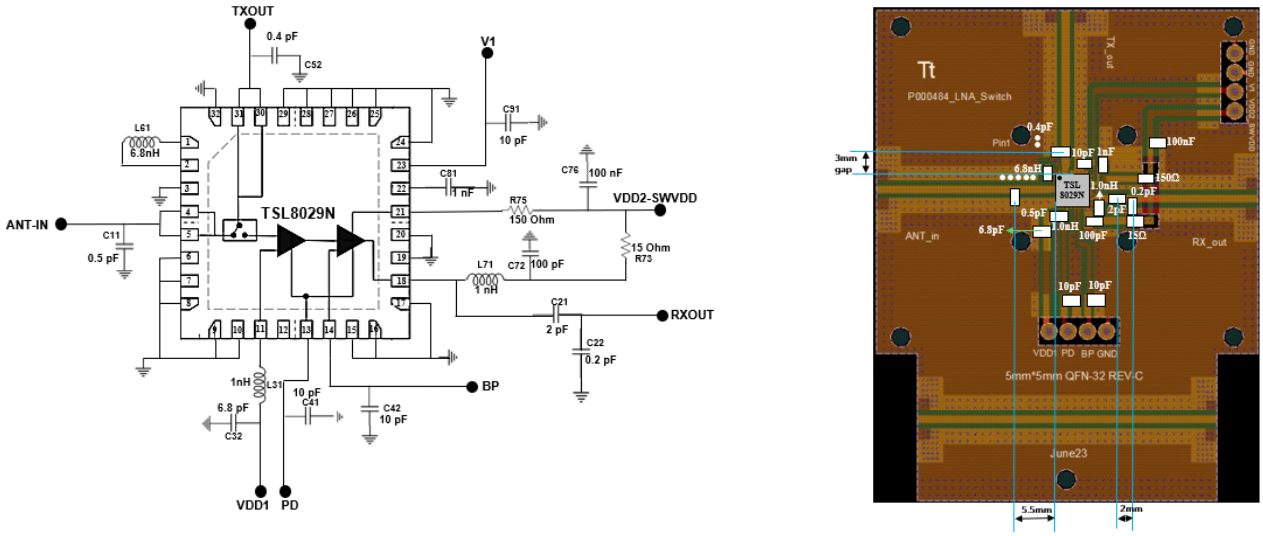

Figure 13: Schematic and layout of the 2900 to 3300 MHz EVB E

Table 19: BOM of the 2900 to 3300 MHz EVB E

Component ID	Value	Manufacturer	Recommended part number	Qty
C11	0.5 pF	Murata	600S0R5BT250XT	1
C21	2 pF	Murata	GJM1555C1H2R0BB01D	1
C22	0.2 pF	Murata	GJM1555C1HR20BB01J	1
L31, L71	1 nH	Coilcraft	0402DC-1N0XJRW	2
C32	6.8 pF	Murata	GJM1555C1H6R8BB01D	1
C41, C42, C91	10 pF	Murata	GJM1555C1H100JB01D	3
C52	0.4 pF	Murata	600S0R4BT250XT	1
L61	3.9 nH	Coilcraft	0402DC-3N9XGRW	1
C72	100 pF	AVX	04025A101JAT4A	1
R73	15 Ω	Panasonic	ERJ-H2RD15R0X	1
R75	150 Ω	Panasonic	ERJ-2RHD1500X	1
C76	100 nF	TDK	C1005X7R1H104K050BE	1
C81	1 nF	Murata	04025C102JAT2A	1
PCB	Rogers RO4350B, 20 mil, 1 oz copper			1

Note: Series cap on ANT and TX ports should have 250 V voltage ratings to handle 100 W power. The heatsink needs to be added at the bottom of this board for proper power spreading.

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Test Procedure

Biasing sequence

To properly bias the TSL8029N-EVB-C, follow these steps:

1. Ground the GND test point.
2. Apply bias to the V_{DD2}/SWV_{DD} and $V_{DD1} = 5$ V test points.
3. Apply bias to the V_1 test point.
4. Apply bias to the BP test points.
5. Apply bias to the PD test point.
6. Apply an RF input signal.

Test set-up

The TSL8029N-EVB-C is shipped fully assembled and tested. Figure 14 illustrates a basic test set-up diagram for evaluating the S-parameters in RX mode, including receive gain, transmit insertion loss and isolation, and RF input and output return losses using a network analyzer. Follow these steps to complete the test set-up and verify the operation of the TSL8029N-EVB-C:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the V_{DD1}, SWV_{DD} and V_{DD2} test points to the voltage output terminal of a 5 V supply that sources a current of approximately 90 mA in receive operation for high gain mode or 4 to 5 mA for power-down mode.
3. Connect the BP, PD, and V_1 test points to the ground terminal of the power supply for high gain receive operation. The TSL8029N-EVB-C can be configured in different modes by connecting the control test points to 5 V or ground, as shown in Table 6 and Table 7.
4. Connect a calibrated network analyzer to the ANT_in, TX_out, and RX_out SMA connectors. Sweep the frequency from 1 GHz to 6 GHz and set the power to -25 dBm.

The TSL8029N-EVB-C is expected to have a high and low receive gain of 33 dB and 14.5 dB respectively at 3.6 GHz. Refer to Typical characteristics for the expected results.

Additional test equipment is required for a comprehensive evaluation of the device's functions and performance.

- For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with a noise option. It is recommended to use a low excess noise ratio (ENR) noise source.
- For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.
- For power compression and power handling evaluations, use a two-channel power meter and a signal generator. Ensure that the input power amplifier has sufficient power capacity. Test accessories such as couplers and attenuators must also have adequate power handling capabilities.

The TSL8029N-EVB-C is equipped with a support plate attached to the bottom side. To ensure optimal heat dissipation and minimize thermal rise during high power evaluations, attach this support plate to a heat sink using thermal grease.

Please note that measurements conducted at the SMA connectors of the TSL8029N-EVB-C include the losses of the SMA connectors and the PCB. The through line should be measured to calibrate the effects of the TSL8029N-EVB-C. The through line consists of an RF input line and an RF output line that are connected to the device and have equal lengths. The through line information is provided in the EVB.

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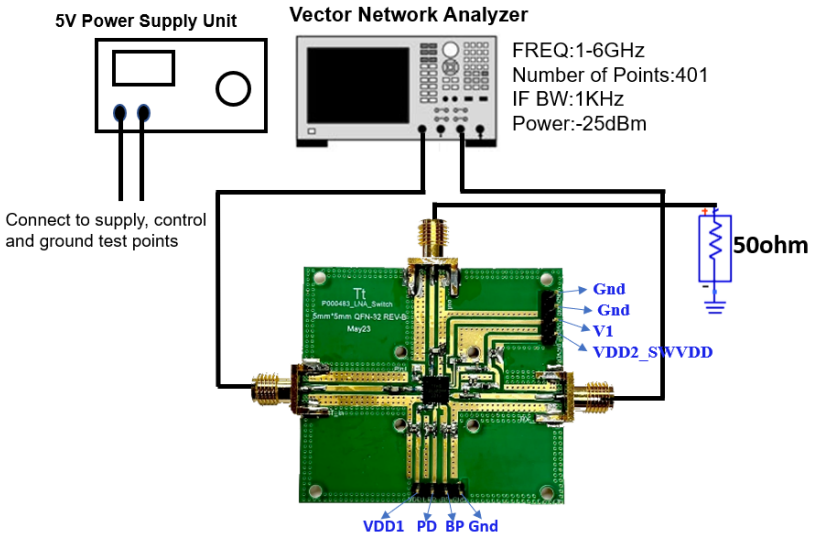

RX mode test set up:

For RX HG apply

- VDD2_SWVDD=5V
- V1=0V
- VDD1 =5V
- BP =0V
- PD=0V

If you change BP=0V to 5V **LG mode** will on
If you change PD=0V to 5V then **PD mode** will on

For TX mode apply

- VDD2_SWVDD=5V
- V1=5V

Do not apply any voltages on VDD1,BP and PD pins

Figure 14: Test set-up diagram for RX mode

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Device Package information

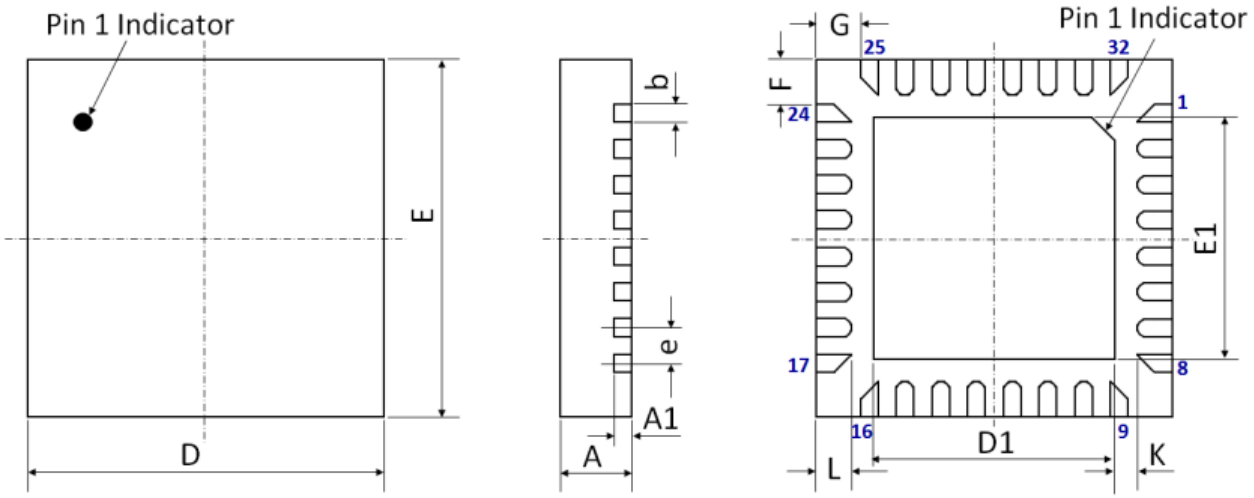

Figure 15: Device package drawing (all dimensions in mm).

Table 20: Device Package Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A	0.85	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	3.2	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	5.00 BSC	±0.05	G	0.625	±0.05
D1	3.2	±0.06	L	0.40	±0.05
e	0.5 BSC	±0.05	K	0.5	±0.05

Lead finish: pure Sn without underlayer; thickness 7.5 μm to 20 μm (typical 10 μm to 12 μm).

Please refer to application notes TN-001 PCB Design guideline and TN-002 Solder Rework at TagoreTech web page for PCB and soldering guidelines.

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PCB Land Design

Guidelines:

1. 4-layer PCB is recommended.
2. Via diameter is recommended to be 0.2 mm to prevent solder wicking inside the vias.
3. Thermal vias shall be placed on the center pad and should be filled/plugged with solder or copper.
4. The maximum via number for the center pad is 5(X) $\times$ 5(Y) $=$ 25.

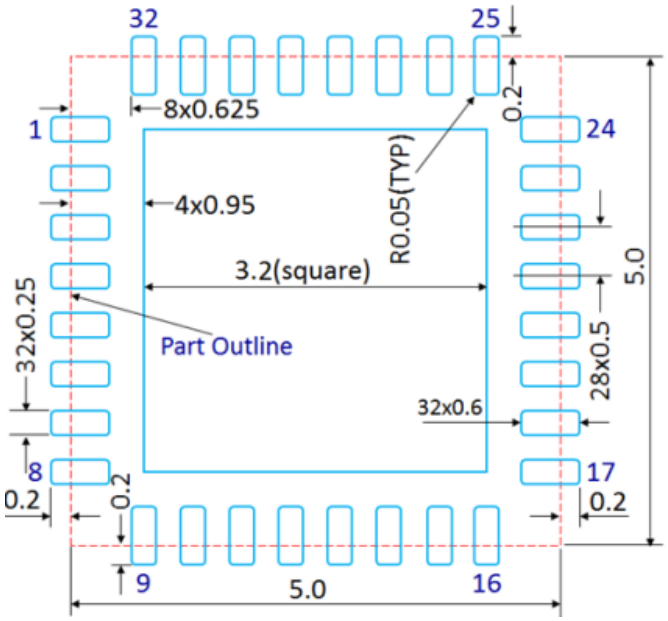

Figure 16: PCB land pattern (dimensions in mm).



Non-solder mask defined (preferred) Solder mask defined

Figure 17: Solder mask pattern (dimensions in mm).

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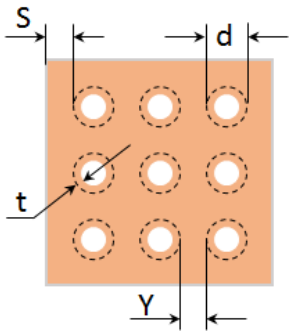

Figure 18: Thermal via pattern (recommended values: S $\geq$ 0.15 mm; Y $\geq$ 0.20 mm; d = 0.3 mm; plating thickness t = 25 μm or 50 μm).

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PCB Stencil Design

Guidelines:

1. Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
2. Stencil thickness is recommended to be 125 μm.

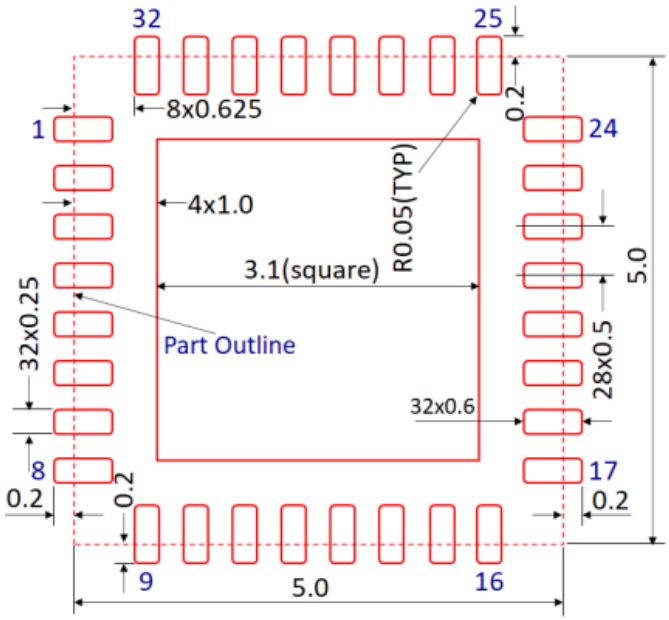

Figure 19: Stencil openings (dimensions in mm).

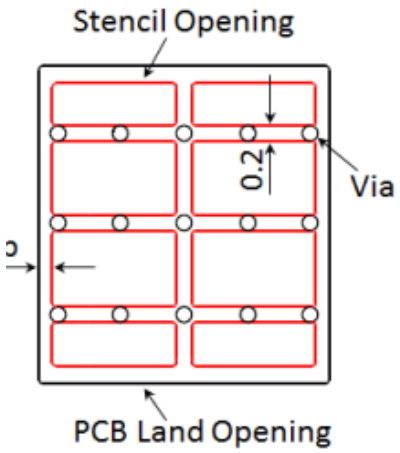

Figure 20: Stencil openings shall not cover via areas if possible (dimensions in mm).

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Tape and Reel Information

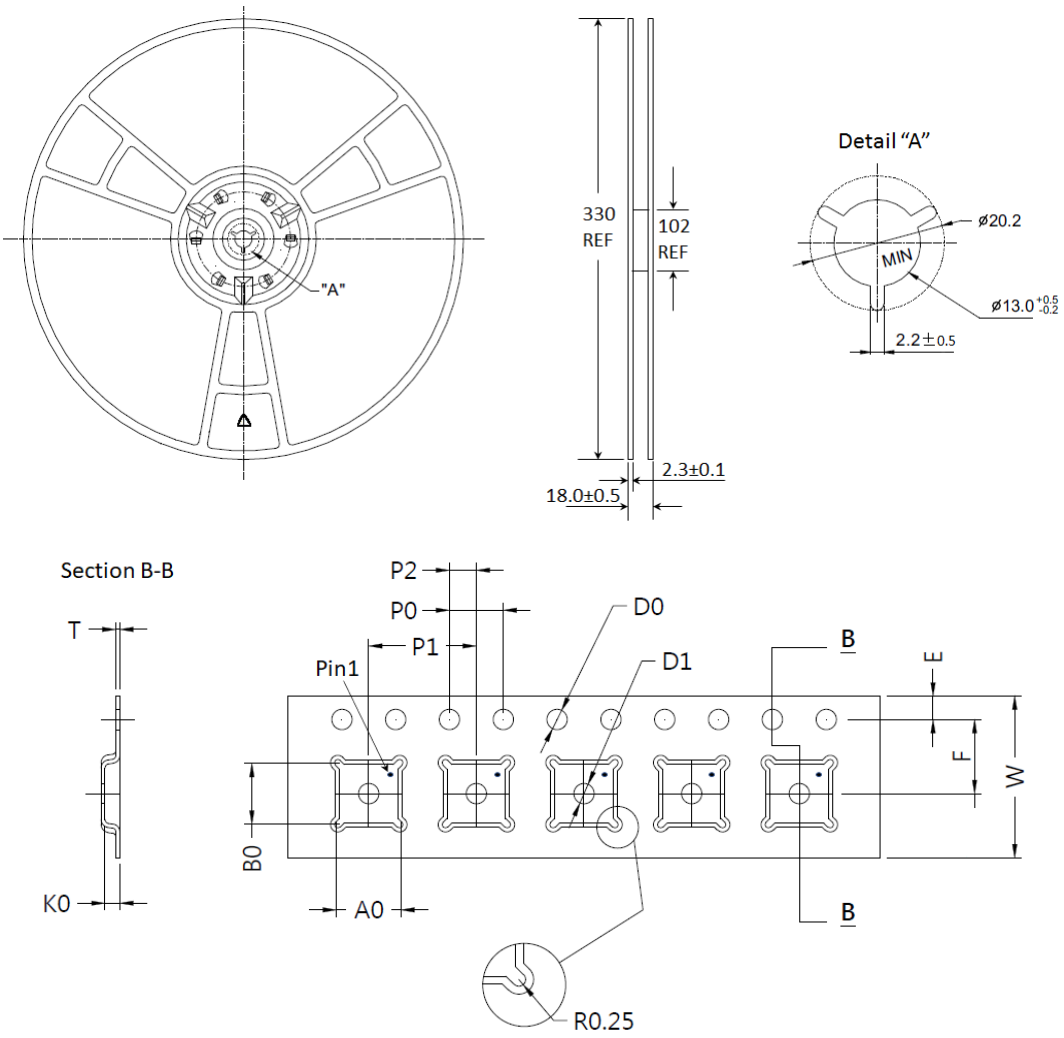

Figure 21: Tape and reel drawing.

Table 21: Tape and Reel Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A0	5.35	±0.10	K0	1.10	±0.10
B0	5.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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Glossary

ANT	Antenna port
BP	Bypass control of the second LNA stage
ENR	Excess noise ratio
EVB	Evaluation board
HG, LG	High gain mode, low gain mode
IL	Insertion loss
LNA	Low noise amplifier
LTE	Long Term Evolution
Mu1	Stability factor μ
NC	Not internally connected
NF	Noise figure
OIP3	Output third-order intercept point
OP1dB	Output power at 1 dB gain compression
PAR	Peak to average ratio
PD	Power-down control of the LNA stages
RX, TX	Receive, transmit port or operation
SDARS	Satellite digital audio radio service

Changelog

Table 22: Changelog

Date	Revision	Notes
07/30/2024	2.4	Word datasheet.
11/05/2026	3.00	Discontinued; replacement part TSL8028N. Transferred to the TagoreTech datasheet format for archiving; content, plots and graphics are unchanged from the Word datasheet revision 2.4. Typographical corrections only: return loss unit dB, PD/BP pin descriptions, EVB E layout caption, test procedure part number and references. Links to the replacement part, application notes TN-001/TN-002, QR code links, glossary.

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TagoreTech is a fabless US semiconductor company specializing in GaN RF solutions: high-power RF switches in unique GaN-on-Si technology, RF power amplifiers in GaN-on-SiC, and reconfigurable front-end solutions — such as tunable power amplifiers and antenna tuning — that combine the two. TagoreTech serves defense, radar, datalink, 5G infrastructure, and public safety markets.

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Replacement part: TSL8028N

The TSL8029N is discontinued. The replacement part is the TSL8028N (2.0 to 5.0 GHz, 100 W TDD receiver front end, SPDT switch and two-stage LNA, 5 × 5 mm QFN-32): TSL8028N Product Page, TSL8028N Datasheet

TSL8029N Product Information

Latest version of TSL8029N datasheet (archive) is available for download: TSL8029N Datasheet

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