Dual Channel 20 W Receiver Front End 2.0 GHz to 4.2 GHz

Discontinued. This datasheet is provided for archiving purposes only. No alternative part is available. Only very few samples are available; please contact TagoreTech: support@tagoretech.com.

Features

- Integrated dual-channel RF front end: 2-stage LNA and GaN SPDT switch
- On-chip bias and matching
- Single-supply operation
- Gain @ 3.6 GHz: 32 dB (high gain mode), 13 dB (low gain mode)
- NF @ 3.6 GHz: 1.0 dB (high gain mode), 0.9 dB (low gain mode)
- OP1dB @ 3.6 GHz: 20 dBm (high gain mode), 10.5 dBm (low gain mode)
- Operating frequency: 2.0 GHz – 4.2 GHz
- High isolation: RXOUT-CHA to RXOUT-CHB 40 dB typical, TERM-CHA to TERM-CHB 55 dB typical
- Insertion loss @ 3600 MHz: 0.45 dB (TX mode)
- High power handling at $T_{CASE} = 105\,^{\circ}C$, full lifetime: LTE average power (9 dB PAR) 43 dBm
- High OIP3 (high gain mode): 35 dBm typical
- Current at 5 V: 90 mA (high gain), 45 mA (low gain), 5 mA (power-down) typical
- Positive logic control
- 6 mm × 6 mm, 40-pin QFN

Applications

- 4G/5G infrastructure radios
- Small cells and cellular repeaters
- Phase array radar
- SDARS

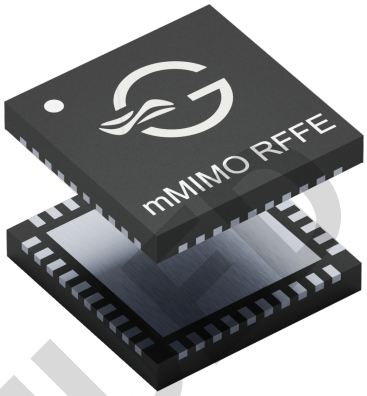


Figure 1: TSL8329M in 6 x 6 x 0.85 mm 40-pin QFN package.

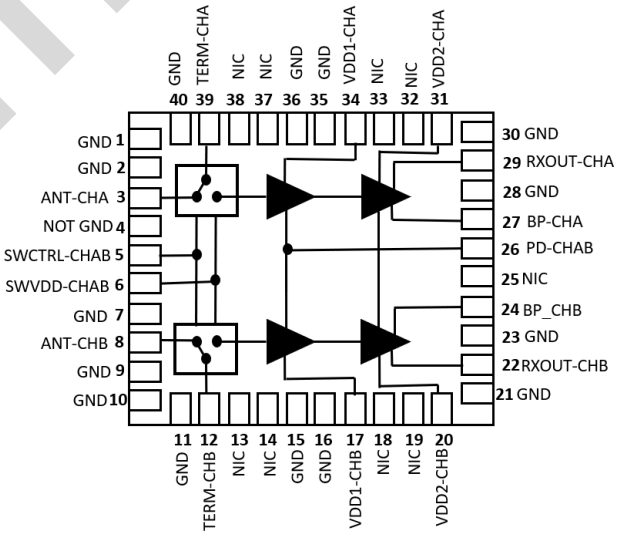


Figure 2: TSL8329M function block diagram (top view).

RoHS/REACH/Halogen free

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General Description

The TSL8329M is a dual-channel, integrated RF front-end multichip module designed for different applications. The device operates from 2.0 GHz to 4.2 GHz. The TSL8329M is configured in dual channels with a cascading two-stage LNA and a high power GaN based SPDT switch.

In high gain mode, the cascaded two-stage LNA and switch offer a low noise figure of 1 dB and a high gain of 32 dB at 3.6 GHz with an output third-order intercept point (OIP3) of 35 dBm (typical). In low gain mode, one stage of the two-stage LNA is in bypass, providing 13 dB of gain at a lower current of 45 mA. In power-down mode, the LNAs are turned off and the device draws 5 mA.

In transmit operation, when the RF inputs are connected to a termination pin (TERM-CHA or TERM-CHB), the switch provides a low insertion loss of 0.45 dB at 3.6 GHz and handles a long-term evolution (LTE) average power (9 dB peak to average ratio (PAR)) of 43 dBm for full lifetime operation.

The device comes in an RoHS compliant, compact, 6 mm × 6 mm, 40-pin QFN.

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Ordering information

Table 1: Ordering Information

Device Part Number	Package Type	Notes
TSL8329M	40-pin 6x6x0.85 mm QFN	Base part number, discontinued
TSL8329MMTRPBF[1]	330 mm (13”) reel, 3 000 pcs	Full reel
TSL8329M-EVB-A	Tuned evaluation board	3300 to 4000 MHz
TSL8329M-EVB-B	Tuned evaluation board	2900 to 3300 MHz
TSL8329M-EVB-C	Tuned evaluation board	2000 to 4000 MHz

[1] MTRPBF - M: Manufacturing, TR: Tape and Reel, and PBF: lead free.
The TSL8329M is discontinued. No alternative part is available. Only very few samples are available; please contact TagoreTech.

Table 2: Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3 000	330 mm (13”)	18 mm

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Pin Assignment

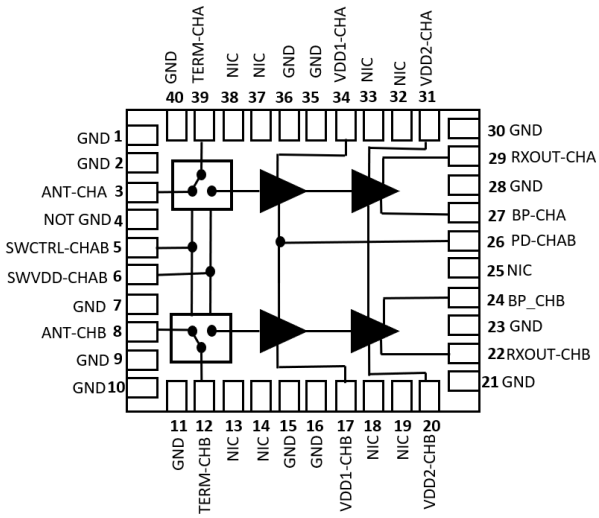


Figure 3: TSL8329M pin assignment and function block diagram [top view]

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Table 3: Pin Definition

Pin Number	Pin Name	Description
1, 2, 7, 9–11, 15, 16, 21, 23, 28, 30, 35, 36, 40	GND	Ground
3	ANT-CHA	RF input to Channel A. The ANT-CHA pin is ac-coupled to 0 V and matched to 50 Ω. Matching and a dc blocking capacitor are not required.
4	NOT GND	Internally used. Do not connect to GND. Leave unconnected.
5	SWCTRL-CHAB	Control voltage for the switches on Channel A and Channel B.
6	SWVDD-CHAB	Supply voltage for the switches on Channel A and Channel B.
8	ANT-CHB	RF input to Channel B. The ANT-CHB pin is ac-coupled to 0 V and matched to 50 Ω. Matching and a dc blocking capacitor are not required.
12	TERM-CHB	Termination output for Channel B. The TERM-CHB pin is the transmitter path for Channel B. The TERM-CHB pin is ac-coupled to 0 V and matched to 50 Ω. No matching and dc blocking capacitor required.
13, 14, 18, 19, 25, 32, 33, 37, 38	NIC	Not internally connected. It is recommended to connect NIC to the RF ground of the PCB.
17	VDD1-CHB	V_{DD1} supplied through an external choke inductor
20	VDD2-CHB	V_{DD2} supplied through an external choke inductor
22	RXOUT-CHB	Receiver output. The RXOUT-CHB pin is the receiver path for Channel B. The RXOUT-CHB pin is ac matched to 50 Ω. No matching component is required. A dc blocking capacitor is required.
24	BP-CHB	Bypass second stage LNA of Channel B.
26	PD-CHAB	Power-down all stages of the LNA for Channel A and Channel B.
27	BP-CHA	Bypass second stage LNA of Channel A.
29	RXOUT-CHA	Receiver output. The RXOUT-CHA pin is the receiver path for Channel A. The RXOUT-CHA pin is ac matched to 50 Ω. No matching component is required. A dc blocking capacitor is required.
31	VDD2-CHA	V_{DD2} supplied through an external choke inductor
34	VDD1-CHA	V_{DD1} supplied through an external choke inductor
39	TERM-CHA	Termination output for Channel A. The TERM-CHA pin is the transmitter path for Channel A. The TERM-CHA pin is ac-coupled to 0 V and matched to 50 Ω. No matching and dc blocking capacitor required.
Package base[1]	Paddle/Slug	DC and RF ground. Also provides thermal relief. Multiple vias are recommended.

[1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heat sinking required.

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings $T_A = +25$°C unless otherwise specified[1].

Parameter	Symbol	Value	Unit
Electrical Ratings			
Supply voltage, VDD1-CHA, VDD1-CHB, VDD2-CHA, VDD2-CHB and SWVDD-CHAB	V_{DD}	+5.5	V
RF input power, transmit input power (average, LTE with 8 dB PAR)	RF_{IN}	43	dBm
RF input power, receive input power (LTE peak, 8 dB PAR)	RF_{IN}	25	dBm
Digital control input voltage, SWCTRL-CHAB, BP-CHA, BP-CHB and PD-CHAB		1.8 to 5.5	V
Digital control input current, SWCTRL-CHAB, BP-CHA, BP-CHB and PD-CHAB		0.2	mA
Storage Temperature Range	T_{st}	−55 – 150	°C
Operating Temperature Range	T_{op}	−40 – 105	°C
Maximum Junction Temperature	T_j	170	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta jc}$	15.0	°C/W
Soldering Temperature	T_{solder}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 – <1000	V
Charged Device Model (CDM)	Level C	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	

[1] Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

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Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Symbol / Condition	Min	Typ	Max	Unit
Drain voltages	VDD1-CHA, VDD1-CHB		+5.0		V
	VDD2-CHA, VDD2-CHB		+5.0		V
Drain bias currents	I_{DQ1}, set by external drain feed		45		mA
	I_{DQ2}, set by external drain feed		90		mA
Switch supply	SWVDD-CHAB		+5		V
Switch control voltages	SWCTRL-CHAB, BP-CHA, BP-CHB, PD-CHAB	0		+5.5	V
RF input power at ANT-CHA, ANT-CHB	PD-CHAB $= 5$ V, BP-CHA $=$ BP-CHB $= 0$ V, 8 dB PAR LTE, full lifetime average			43	dBm
	PD-CHAB $= 0$ V, BP-CHA $=$ BP-CHB $= 0$ V, 8 dB PAR LTE, full lifetime average			31	dBm
	PD-CHAB $= 0$ V, BP-CHA $=$ BP-CHB $= 5$ V, 8 dB PAR LTE, full lifetime average			43	dBm
Digital input SWCTRL-CHAB, PD-CHAB	Low, V_{IL}	0		0.2	V
	High, V_{IH}	0.9		V_{DD}	V
Digital input BP-CHA, BP-CHB	Low, V_{IL}	0		0.2	V
	High, V_{IH}	0.9		V_{DD}	V
Digital input currents	SWCTRL-CHAB, 5 V per channel			$<$7.5	μA
	PD-CHAB, 5 V per channel			200	μA
	BP-CHA, BP-CHB, 5 V per channel			100	μA
Switch control maximum current				7.5	μA
Operating temperature range	T_{op}	-40	+25	+105	°C

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RF Electrical Specifications

VDD1-CHA, VDD1-CHB, VDD2-CHA, VDD2-CHB and SWVDD-CHAB $= 5$ V, SWCTRL-CHAB $= 0$ V or SWVDD-CHAB, BP-CHA $=$ VDD1-CHA or 0 V, BP-CHB $=$ VDD1-CHB or 0 V, PD-CHAB $= 0$ V or VDD1-CHA, $T_{CASE} = +25$°C, 50 Ω system, unless otherwise noted.

Table 6: RF Electrical Specifications, 3300 to 4000 MHz EVB A, $T_{CASE} = +25$°C, $V_{DD} = 5$ V, 50 Ω system.

Parameter	Test Condition	Min	Typ	Max	Unit
Operational frequency range		3.3	3.6	4.0	GHz
Gain	LNAs on, bypass off (high gain)		32		dB
	LNA1 on, bypass on (low gain)		13		dB
Noise figure (de-embedded)	LNAs on, bypass off (high gain)		1		dB
	LNA1 on, bypass on (low gain)		0.9		dB
EVB noise figure	LNAs on, bypass off (high gain)		1.4		dB
	LNA1 on, bypass on (low gain)		1.3		dB
Input return loss	LNAs on, bypass off (high gain)		10		dB
	LNA1 on, bypass on (low gain)		5		dB
Output return loss	LNAs on, bypass off (high gain)		11		dB
	LNA1 on, bypass on (low gain)		9		dB
OP1dB	LNAs on, bypass off (high gain)		20		dBm
	LNA1 on, bypass on (low gain)		10.5		dBm
OIP3	LNAs on, bypass off (high gain), 0 dBm per tone, tone spacing 1 MHz		35		dBm
	LNA1 on, bypass on (low gain), -2 dBm per tone, tone spacing 1 MHz		18		dBm
Current, I_d	LNAs on, bypass off (high gain)		90		mA
	LNA1 on, bypass on (low gain)		45		mA
	PD mode on (both LNAs off)		5		mA
Insertion loss	Transmit operation at 3.6 GHz		0.45		dB
Channel to channel isolation, RXOUT-CHA to RXOUT-CHB	At 3.6 GHz, receive operation		40		dB
Channel to channel isolation, TERM-CHA to TERM-CHB	Transmit operation		55		dB
Switch isolation, ANT-CHA to TERM-CHA and ANT-CHB to TERM-CHB	Transmit operation, PD-CHAB $= 0$ V		25		dB
Switching time (t_{ON}, t_{OFF})	50 % control voltage to 90 %, 10 % of RXOUT-CHA or RXOUT-CHB in receive operation		400		ns
	50 % control voltage to 90 %, 10 % of TERM-CHA or TERM-CHB in transmit operation		400		ns

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Table 7: RF Electrical Specifications, 2900 to 3300 MHz EVB B, $T_{CASE} = +25$°C, $V_{DD} = 5$ V, 50 Ω system.

Parameter	Test Condition	Min	Typ	Max	Unit
Operational frequency range		2.9	3.1	3.3	GHz
Gain[1]	LNAs on, bypass off (high gain)		38 – 35		dB
	LNA1 on, bypass on (low gain)		15 – 13.5		dB
Noise figure (de-embedded)[1]	LNAs on, bypass off (high gain)		0.9 – 1		dB
	LNA1 on, bypass on (low gain)		0.9 – 1		dB
EVB noise figure[1]	LNAs on, bypass off (high gain)		1.4 – 1.3		dB
	LNA1 on, bypass on (low gain)		1.4 – 1.3		dB
Input return loss[1]	LNAs on, bypass off (high gain)		9 – 9.5		dB
	LNA1 on, bypass on (low gain)		9 – 10		dB
Output return loss[1]	LNAs on, bypass off (high gain)		11 – 17		dB
	LNA1 on, bypass on (low gain)		4 – 5.4		dB
OP1dB[1]	LNAs on, bypass off (high gain)		17 – 18		dBm
	LNA1 on, bypass on (low gain)		10 – 11		dBm
OIP3[1]	LNAs on, bypass off (high gain), 0 dBm per tone, tone spacing 1 MHz		32.5 – 30		dBm
	LNA1 on, bypass on (low gain), -2 dBm per tone, tone spacing 1 MHz		25 – 20		dBm
Current, I_d	LNAs on, bypass off (high gain)		90		mA
	LNA1 on, bypass on (low gain)		45		mA
	PD mode on (both LNAs off)		5		mA
Insertion loss	Transmit operation at 3.1 GHz		0.45		dB
Channel to channel isolation, RXOUT-CHA to RXOUT-CHB	At 3.1 GHz, receive operation		35		dB
Channel to channel isolation, TERM-CHA to TERM-CHB	Transmit operation		55		dB
Switch isolation, ANT-CHA to TERM-CHA and ANT-CHB to TERM-CHB	Transmit operation, PD-CHAB $= 0$ V		30		dB
Switching time (t_{ON}, t_{OFF})	50 % control voltage to 90 %, 10 % of RXOUT-CHA or RXOUT-CHB in receive operation		400		ns
	50 % control voltage to 90 %, 10 % of TERM-CHA or TERM-CHB in transmit operation		400		ns

[1] Typical values given as a range over the operational frequency range of the EVB, as in the source datasheet.

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Table 8: RF Electrical Specifications, 2000 to 4000 MHz EVB C, $T_{CASE} = +25$°C, $V_{DD} = 5$ V, 50 Ω system.

Parameter	Test Condition	Min	Typ	Max	Unit
Operational frequency range		2.0	3.0	4.0	GHz
Gain[1]	LNAs on, bypass off (high gain)		37 – 29		dB
	LNA1 on, bypass on (low gain)		18 – 12		dB
Noise figure (de-embedded)[1]	LNAs on, bypass off (high gain)		0.7 – 1.2		dB
	LNA1 on, bypass on (low gain)		0.7 – 1.2		dB
EVB noise figure[1]	LNAs on, bypass off (high gain)		1.1 – 1.6		dB
	LNA1 on, bypass on (low gain)		1.1 – 1.6		dB
Input return loss[1]	LNAs on, bypass off (high gain)		7.3 – 3.3		dB
	LNA1 on, bypass on (low gain)		4.2 – 7.3		dB
Output return loss[1]	LNAs on, bypass off (high gain)		4 – 17		dB
	LNA1 on, bypass on (low gain)		3 – 24		dB
OP1dB[1]	LNAs on, bypass off (high gain)		18.5 – 20.5		dBm
	LNA1 on, bypass on (low gain)		7 – 12		dBm
OIP3[1]	LNAs on, bypass off (high gain), 0 dBm per tone, tone spacing 1 MHz		31 – 35		dBm
	LNA1 on, bypass on (low gain), -2 dBm per tone, tone spacing 1 MHz		17 – 21		dBm
Current, I_d	LNAs on, bypass off (high gain)		90		mA
	LNA1 on, bypass on (low gain)		45		mA
	PD mode on (both LNAs off)		5		mA
Insertion loss	Transmit operation at 3.0 GHz		0.45		dB
Channel to channel isolation, RXOUT-CHA to RXOUT-CHB	At 3.0 GHz, receive operation		35		dB
Channel to channel isolation, TERM-CHA to TERM-CHB	Transmit operation		55		dB
Switch isolation, ANT-CHA to TERM-CHA and ANT-CHB to TERM-CHB	Transmit operation, PD-CHAB $= 0$ V		30		dB
Switching time (t_{ON}, t_{OFF})	50 % control voltage to 90 %, 10 % of RXOUT-CHA or RXOUT-CHB in receive operation		400		ns
	50 % control voltage to 90 %, 10 % of TERM-CHA or TERM-CHB in transmit operation		400		ns

[1] Typical values given as a range over the operational frequency range of the EVB, as in the source datasheet.

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Truth Tables

Table 9: Truth Table: Switch Control

SWCTRL-CHAB	Signal path select	
	Transmit operation	Receive operation
Low	Off	On
High	On	Off

Table 10: Truth Table: Receive Operation

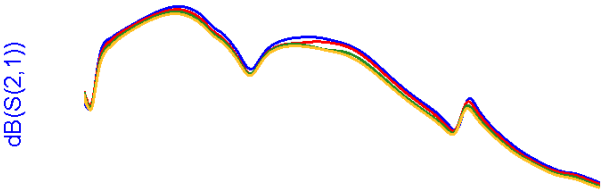
Receive operation	PD-CHAB	BP-CHA, BP-CHB	Signal path
High gain mode	Low	Low	ANT-CHA to RXOUT-CHA, ANT-CHB to RXOUT-CHB
Low gain mode	Low	High	ANT-CHA to RXOUT-CHA, ANT-CHB to RXOUT-CHB
Power-down high isolation mode	High	Low	ANT-CHA to RXOUT-CHA, ANT-CHB to RXOUT-CHB
Power-down low isolation mode	High	High	ANT-CHA to RXOUT-CHA, ANT-CHB to RXOUT-CHB

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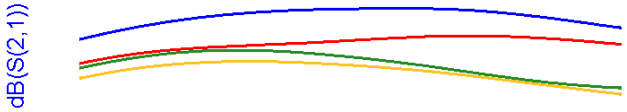
Typical characteristics

Measured on the 3.3 to 4.0 GHz tuned EVB A at -40°C, $+25$°C, $+85$°C and $+105$°C.

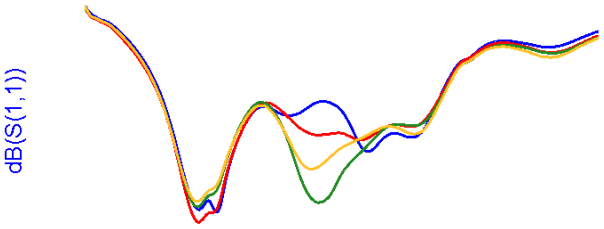
Receive operation, low gain mode



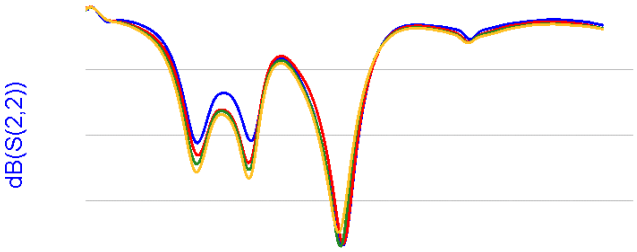
S21 (gain) vs frequency



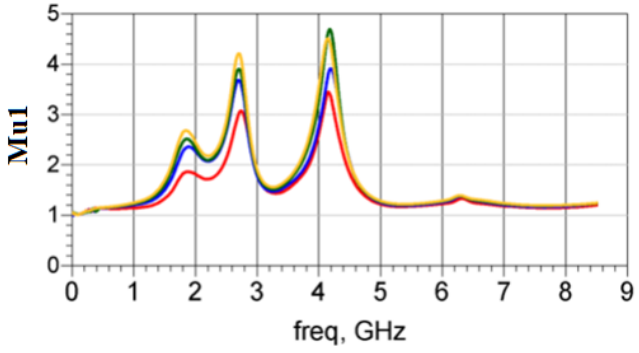
S21 (gain) vs frequency, 3.2 to 4.1 GHz



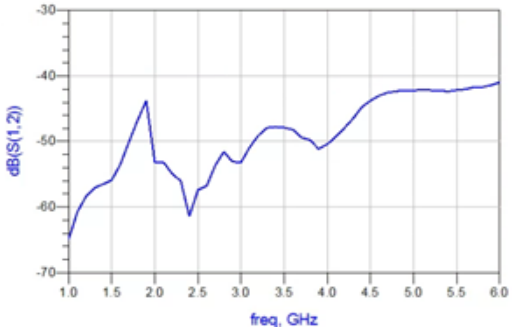
S11 (input return loss) vs frequency



S22 (output return loss) vs frequency

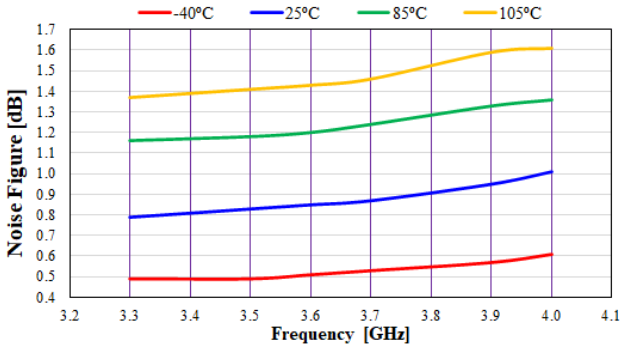


Mu1 vs frequency

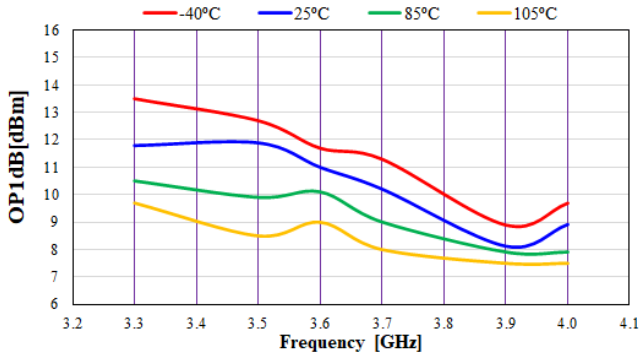


Channel to channel isolation vs frequency

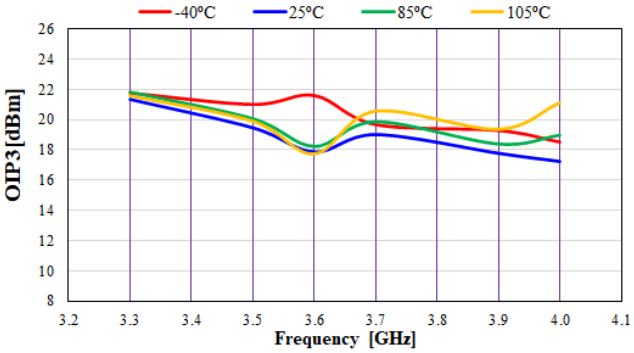
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NF (de-embedded) vs frequency



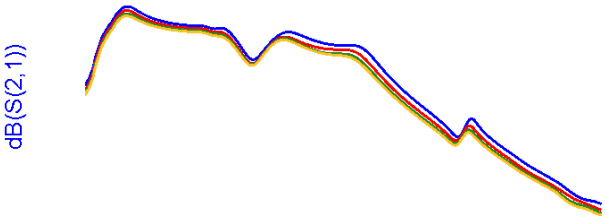
OP1dB vs frequency



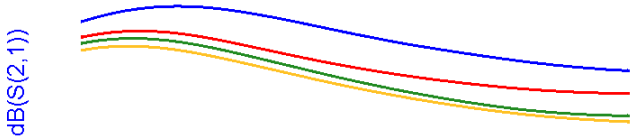
OIP3 vs frequency

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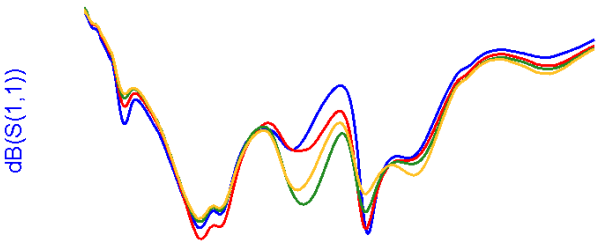
Receive operation, high gain mode



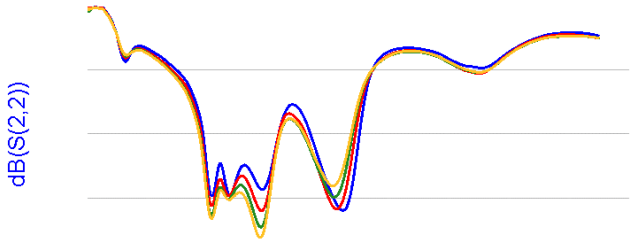
S21 (gain) vs frequency



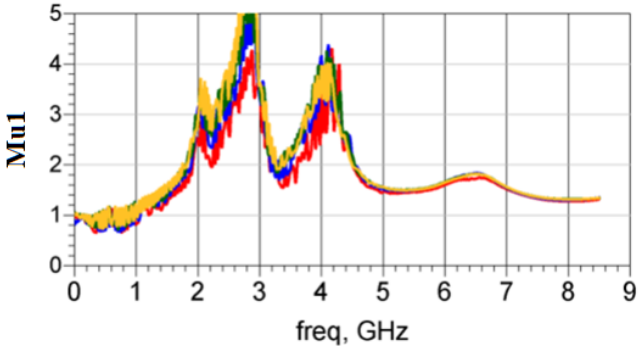
S21 (gain) vs frequency, 3.2 to 4.1 GHz



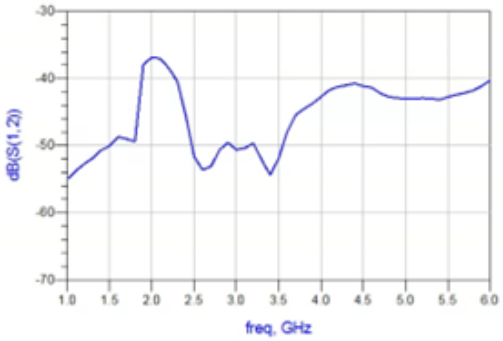
S11 (input return loss) vs frequency



S22 (output return loss) vs frequency

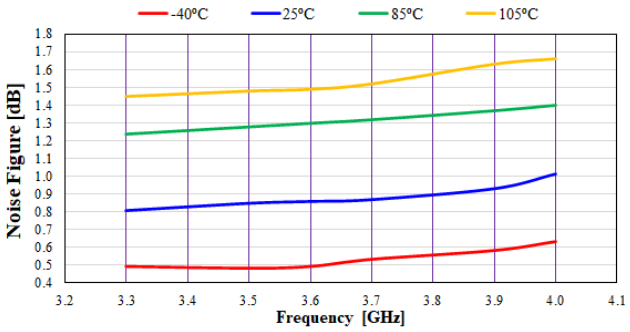


Mu1 vs frequency

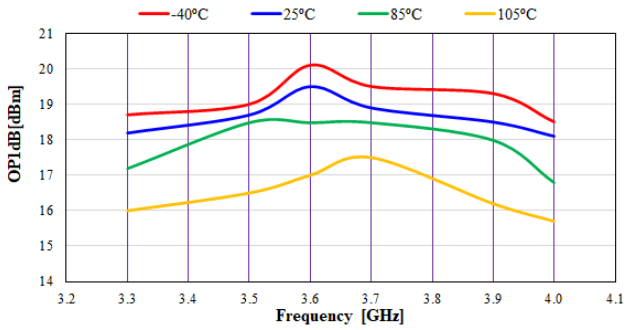


Channel to channel isolation vs frequency

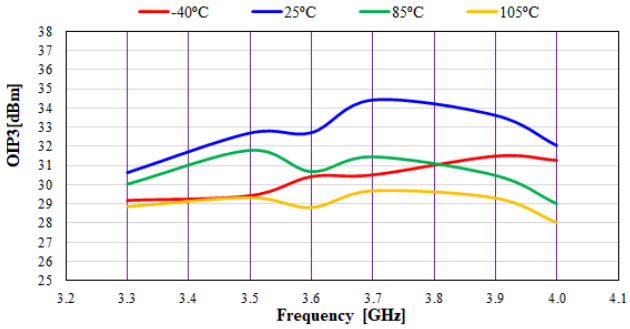
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NF (de-embedded) vs frequency



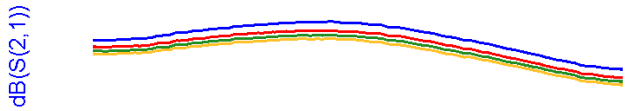
OP1dB vs frequency



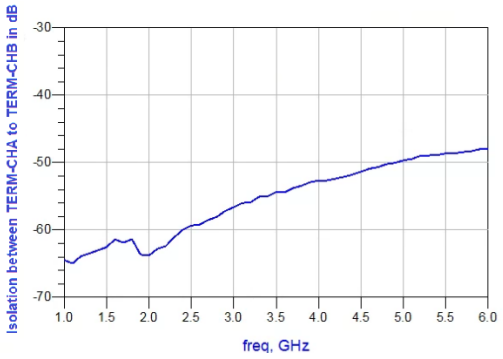
OIP3 vs frequency

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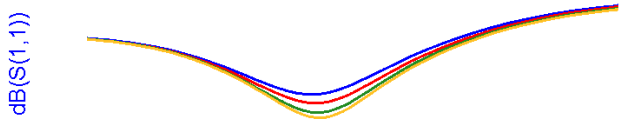
Transmit operation



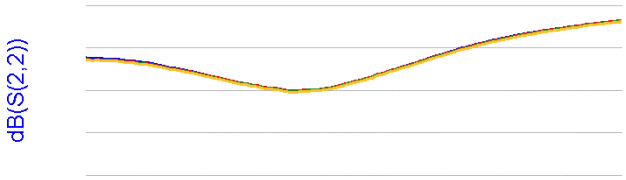
Insertion loss vs frequency



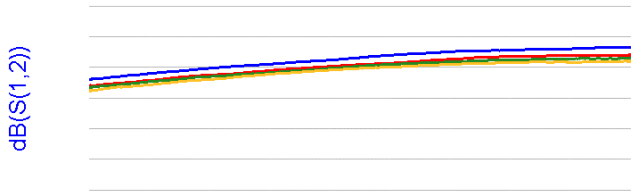
TERM-CHA to TERM-CHB isolation vs frequency



Input return loss vs frequency



Output return loss vs frequency



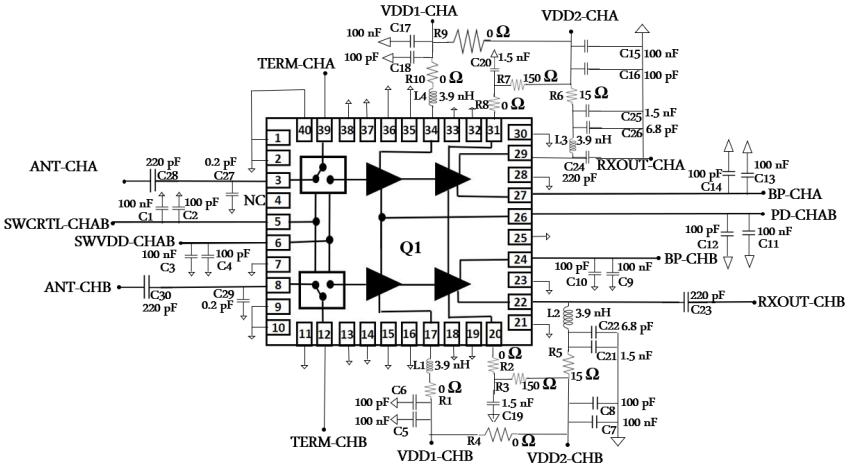
ANT to TERM isolation vs frequency, LNA on

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Evaluation Boards

3300 to 4000 MHz EVB A

RF electrical specifications in Table 6.



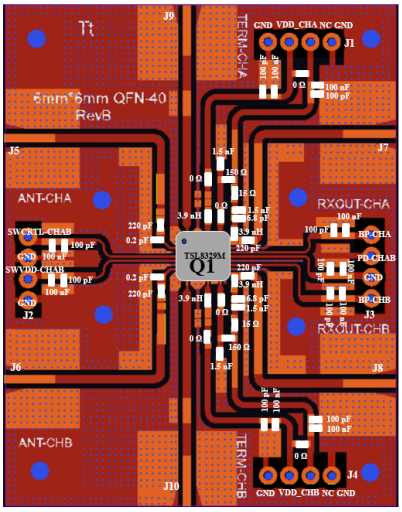


Figure 9: Schematic and layout of the 3300 to 4000 MHz EVB A

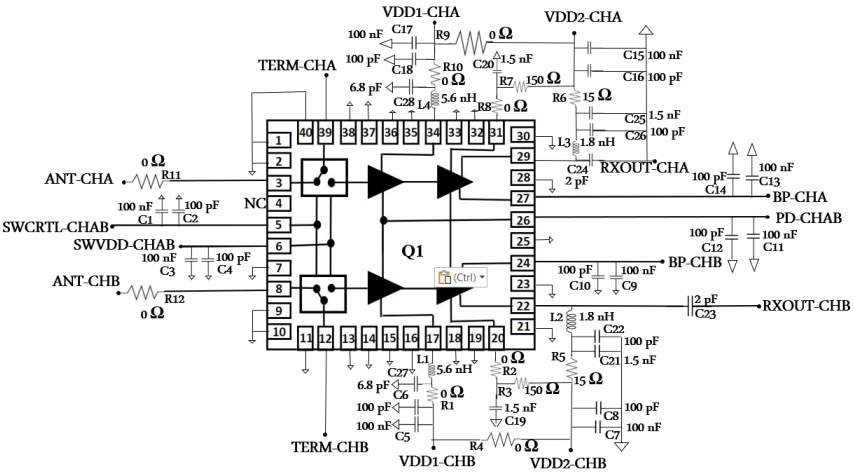
Table 11: BOM of the 3300 to 4000 MHz EVB A

Component ID	Value	Manufacturer	Recommended part number	Qty
R1, R2, R4, R8, R9, R10	0 Ω	Panasonic	ERJ-2GE0R00X	6
R3, R7	150 Ω	Panasonic	ERJ-2RHD1500X	2
R5, R6	15 Ω	Panasonic	ERJ-H2RD15R0X	2
L1, L2, L3, L4	3.9 nH	Coilcraft / Wurth Electronics	0402HP-3N9XGRW / 744916039	4
C22, C26	6.8 pF	Murata	GJM1555C1H6R8BB01D	2
C19, C20, C21, C25	1.5 nF	Murata	04025C152JAT2A	4
C23, C24, C28, C30	220 pF	Kemet	C0402C221K5GACAUTO	4
C27, C29	0.2 pF	Murata	GJM1555C1HR20BB01D	2
C2, C4, C6, C8, C10, C12, C14, C16, C18	100 pF	AVX	04025A101JAT4A	9
C1, C3, C5, C7, C9, C11, C13, C15, C17	100 nF	TDK	C1005X7R1H104K050BE	9
Q1	GaAs LNA + GaN switch	TagoreTech	TSL8329M	1
PCB	Rogers RO4350B, 20 mil, 1 oz copper			1

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2900 to 3300 MHz EVB B

RF electrical specifications in Table 7.



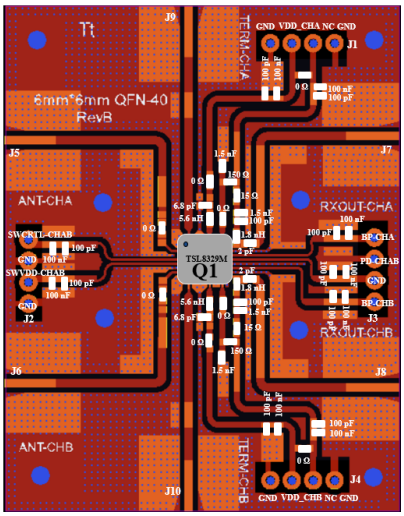


Figure 10: Schematic and layout of the 2900 to 3300 MHz EVB B

Table 12: BOM of the 2900 to 3300 MHz EVB B

Component ID	Value	Manufacturer	Recommended part number	Qty
R1, R2, R4, R8, R9, R10, R11, R12	0 Ω	Panasonic	ERJ-2GE0R00X	8[1]
R3, R7	150 Ω	Panasonic	ERJ-2RHD1500X	2
R5, R6	15 Ω	Panasonic	ERJ-H2RD15R0X	2
L2, L3	1.8 nH	Coilcraft / Wurth Electronics	0603HP-1N8XJLW / 744761018A	2
L1, L4	5.6 nH	Coilcraft / Wurth Electronics	0402HP-5N6XGRW / 744916056	2
C27, C28	6.8 pF	Murata	GJM1555C1H6R8BB01D	2
C19, C20, C21, C25	1.5 nF	Murata	04025C152JAT2A	4
C23, C24	2 pF	Murata	GJM1555C1H2R0BB01D	2
C2, C4, C6, C8, C10, C12, C14, C16, C18, C22, C26	100 pF	AVX	04025A101JAT4A	11[1]
C1, C3, C5, C7, C9, C11, C13, C15, C17	100 nF	TDK	C1005X7R1H104K050BE	9
Q1	GaAs LNA + GaN switch	TagoreTech	TSL8329M	1
PCB	Rogers RO4350B, 20 mil, 1 oz copper			1

[1] Quantity corrected to the number of listed component IDs (the source datasheet gives 6 and 9).

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2000 to 4000 MHz EVB C

RF electrical specifications in Table 8.

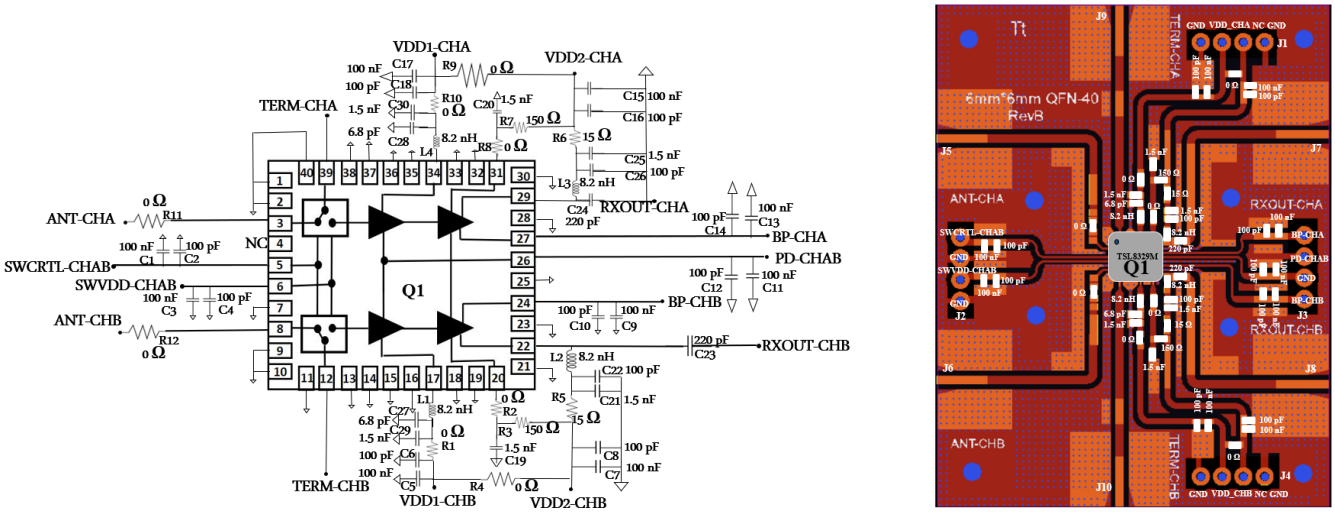


Figure 11: Schematic and layout of the 2000 to 4000 MHz EVB C

Table 13: BOM of the 2000 to 4000 MHz EVB C

Component ID	Value	Manufacturer	Recommended part number	Qty
R1, R2, R4, R8, R9, R10, R11, R12	0 Ω	Panasonic	ERJ-2GE0R00X	8
R3, R7	150 Ω	Panasonic	ERJ-2RHD1500X	2
R5, R6	15 Ω	Panasonic	ERJ-H2RD15R0X	2
L1, L2, L3, L4	8.2 nH	Coilcraft / Wurth Electronics	0402HP-8N2XGRW / 744916082	4[1]
C27, C28	6.8 pF	Murata	GJM1555C1H6R8BB01D	2
C19, C20, C21, C25, C29, C30	1.5 nF	Murata	04025C152JAT2A	6
C23, C24	220 pF	Kemet[2]	C0402C221K5GACAUTO	2
C2, C4, C6, C8, C10, C12, C14, C16, C18, C22, C26	100 pF	AVX	04025A101JAT4A	11
C1, C3, C5, C7, C9, C11, C13, C15, C17	100 nF	TDK	C1005X7R1H104K050BE	9
Q1	GaAs LNA + GaN switch	TagoreTech	TSL8329M	1
PCB	Rogers RO4350B, 20 mil, 1 oz copper			1

[1] Quantity corrected to the number of listed component IDs (the source datasheet gives 2).
[2] Manufacturer corrected to match the part number (Kemet, as in EVB A); the source datasheet gives Murata.

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Test Procedures

EVB test details

Table 14: RF and DC Connector Details

Connector name and type	Voltage / signal name	Description
J1, DC header	VDD-CHA	Supply LNA on Channel A
J2, DC header	SWVDD-CHAB, SWCTRL-CHAB	Supply switches on Channel A and Channel B; control switches on Channel A and Channel B
J3, DC header	BP-CHA, BP-CHB, PD-CHAB	Bypass LNA stage 2 on Channel A; bypass LNA stage 2 on Channel B; power down all LNA stages on Channel A and B
J4, DC header	VDD-CHB	Supply LNA on Channel B
J5, RF connector	ANT-CHA	Antenna input to Channel A
J6, RF connector	ANT-CHB	Antenna input to Channel B
J7, RF connector	RXOUT-CHA	Receiver output from Channel A
J8, RF connector	RXOUT-CHB	Receiver output from Channel B
J9, RF connector	TERM-CHA	Termination output from Channel A
J10, RF connector	TERM-CHB	Termination output from Channel B

All connector and header names are given in the EVB layout figures.

Biasing sequence

To bias up the TSL8329M-EVB-A for Channel A, perform the following steps:

1. Ground the GND or GND1 test point.
2. Bias up the SWVDD-CHAB $= 5$ V test points.
3. Bias up the SWCTRL-CHAB test point.
4. Bias up the VDD-CHA test point.
5. Bias up the BP-CHA test points.
6. Bias up the PD-CHAB test point.
7. Apply an RF input signal.

Test set-up

The TSL8329M-EVB-A is shipped fully assembled and tested. Figure 12 provides a basic test set-up diagram to evaluate the S-parameters in RX mode to get the Channel A performance (receive gain, transmit insertion loss and isolation, RF input and output return losses) using a network analyzer. Perform the following steps to complete the test set-up and verify the operation of the TSL8329M-EVB-A:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD-CHA and SWVDD-CHAB test points to the voltage output terminal of the 5 V supply that sources a current of approximately 90 mA in receive operation for high gain mode or 5 mA for power-down mode.
3. Connect the BP-CHA, BP-CHB, PD-CHAB, and SWCTRL-CHAB test points to the ground terminal of the power supply for high gain receive operation. The TSL8329M-EVB-A can be configured in different modes by connecting the control test points to 5 V or ground, as shown in Table 9 and Table 10.
4. Connect a calibrated network analyzer to the ANT-CHA, TERM-CHA, and RXOUT-CHA SMA connectors. Sweep the frequency from 1 GHz to 6 GHz and set the power to -25 dBm.
5. Connect 50 Ω loads to the ANT-CHB, TERM-CHB, and RXOUT-CHB SMA connectors.

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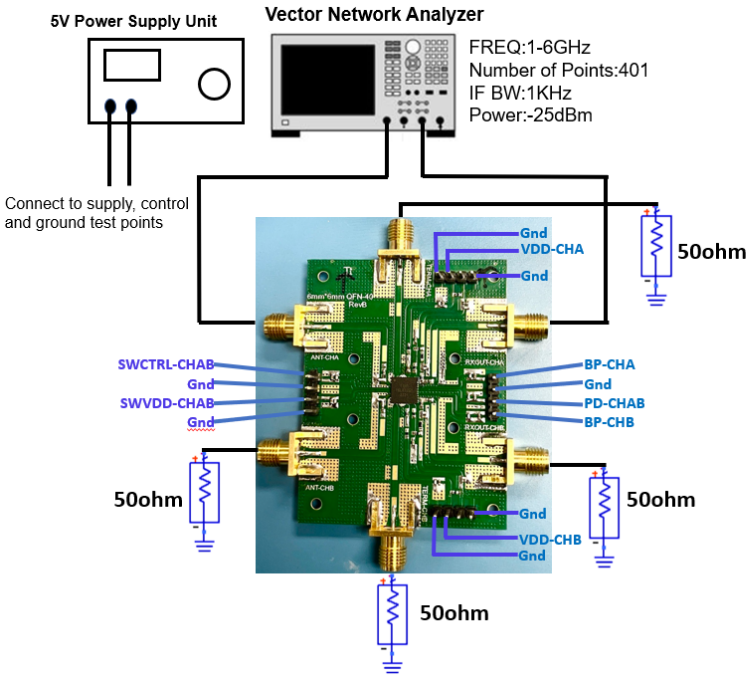
6. The TSL8329M-EVB-A is expected to have a high and low receive gain of 32 dB and 13 dB respectively, at 3.6 GHz. See the expected results in Typical characteristics.

Additional test equipment is needed to fully evaluate the device functions and performance.

- For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with noise option. The use of a low excess noise ratio (ENR) noise source is recommended.
- For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.
- For power compression and power handling evaluations, use a two-channel power meter and a signal generator. A power amplifier with great enough power is recommended at the input. Test accessories such as couplers and attenuators must have enough power handling.

The TSL8329M-EVB-A comes with a support plate attached to the bottom side. To ensure maximum heat dissipation and to reduce thermal rise on the TSL8329M-EVB-A during high power evaluations, this support plate must be attached to a heat sink using thermal grease.

Note that the measurements performed at the SMA connectors of the TSL8329M-EVB-A include the losses of the SMA connectors and the PCB. The through line must be measured to calibrate out the TSL8329M-EVB-A effects. The through line is the summation of an RF input line and an RF output line that are connected to the device and equal in length.



RX mode test set up:

For RX HG for Channel A apply

- SWVDD-CHAB=5V
- SWCTRL-CHAB=0V
- VDD-CHA =5V
- BP-CHA =0V
- PD-CHAB =0V
- Do not apply any voltage on VDD-CHB,BP-CHB pins

If you change BP-CHA=0V to 5V **LG mode** will on
If you change PD-CHAB=0V to 5V then **PD mode** will on

For RX HG for Channel B apply

- SWVDD-CHAB=5V
- SWCTRL-CHAB=0V
- VDD-CHB =5V
- BP-CHB =0V
- PD-CHAB =0V
- Do not apply any voltage on VDD-CHA,BP-CHA pins

If you change BP-CHB=0V to 5V **LG mode** will on
If you change PD-CHAB=0V to 5V then **PD mode** will on

For TX mode for Channel A/B apply

- SWVDD-CHAB=5V
- SWCTRL-CHAB=5V
- Do not apply any voltages on VDD-CHA,VDD-CHB, BP-CHA,BP-CHB and PD-CHAB pins

Figure 12: Test set-up diagram for RX mode

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Device Package information

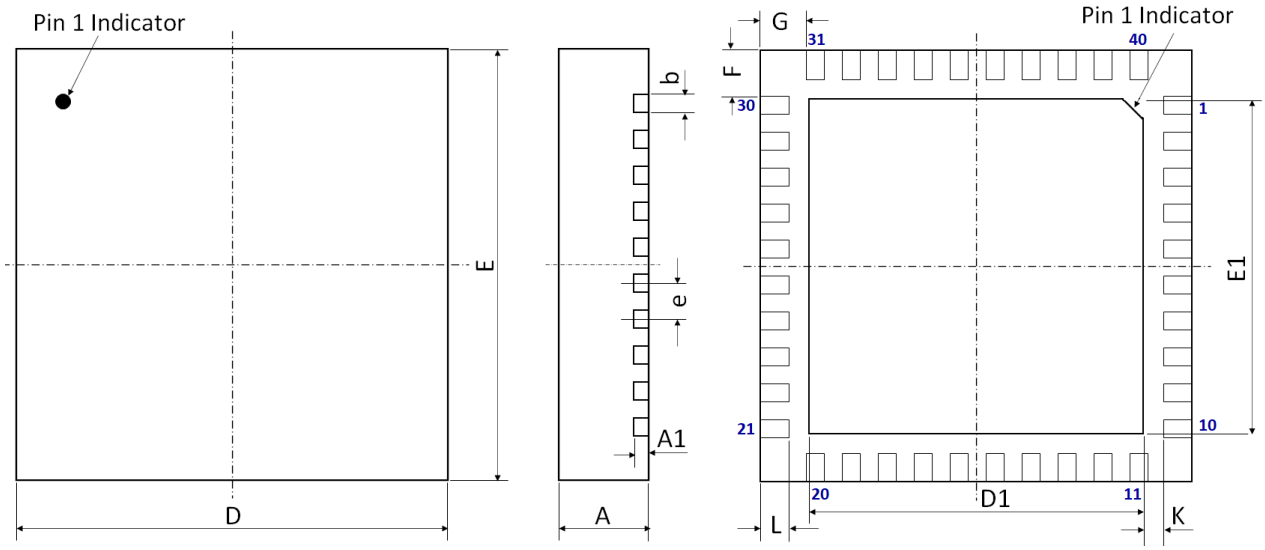


Figure 13: Device package drawing (all dimensions in mm).

Table 15: Device Package Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A	0.85	±0.05	E	6.00 BSC	±0.05
A1	0.203	±0.02	E1	4.65	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	6.00 BSC	±0.05	G	0.625	±0.05
D1	4.65	±0.06	L	0.40	±0.05
e	0.50 BSC	±0.05	K	0.275	±0.05

Lead finish: pure Sn without underlayer; thickness 7.5 μm to 20 μm (typical 10 μm to 12 μm).

Please refer to application notes TN-001 PCB Design guideline and TN-002 Solder Rework at TagoreTech web page for PCB and soldering guidelines.

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PCB Land Design

Guidelines:

1. 4-layer PCB is recommended.
2. Via diameter is recommended to be 0.3 mm to prevent solder wicking inside the vias.
3. Thermal vias shall be placed on the center pad and should be filled/plugged with solder or copper.
4. The maximum via number for the center pad is 9(X) $\times$ 9(Y) $=$ 81.

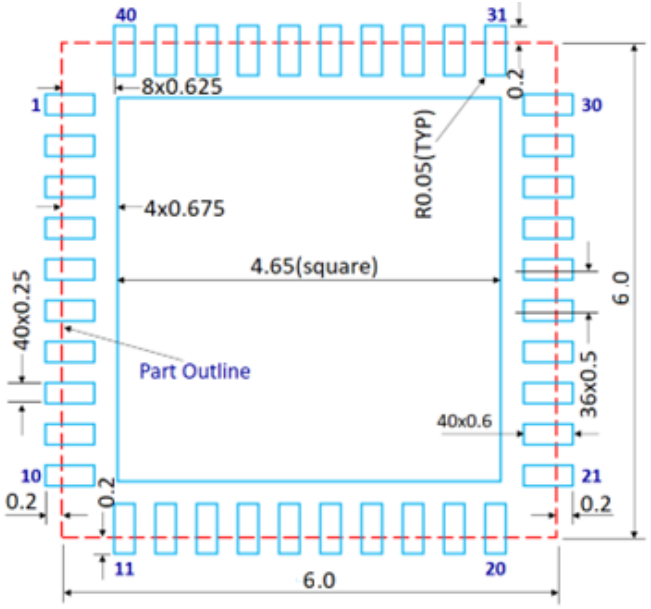


Figure 14: PCB land pattern (dimensions in mm).



Figure 15: Solder mask pattern (dimensions in mm).

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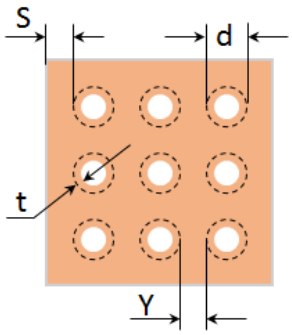


Figure 16: Thermal via pattern (recommended values: S $\geq$ 0.15 mm; Y $\geq$ 0.20 mm; d = 0.3 mm; plating thickness t = 25 μm or 50 μm).

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PCB Stencil Design

Guidelines:

1. Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
2. Stencil thickness is recommended to be 125 μm.

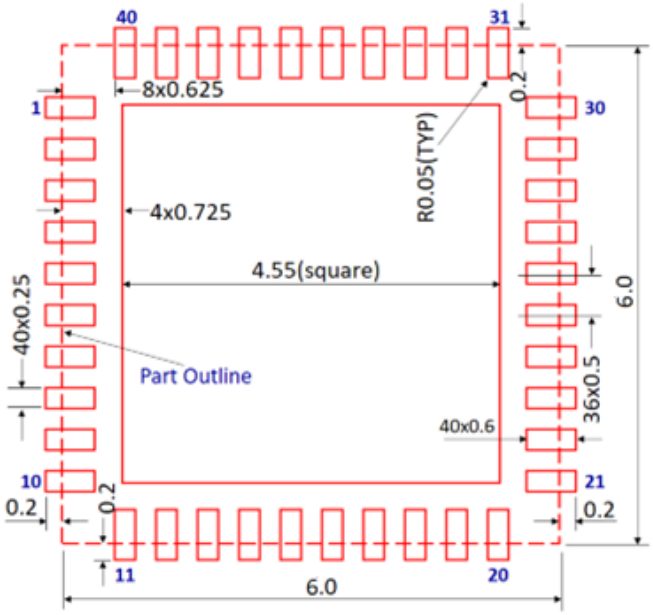


Figure 17: Stencil openings (dimensions in mm).

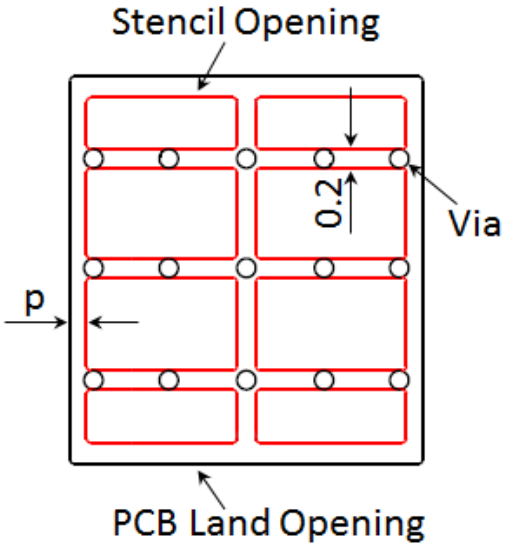


Figure 18: Stencil openings shall not cover via areas if possible (dimensions in mm).

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Tape and Reel Information

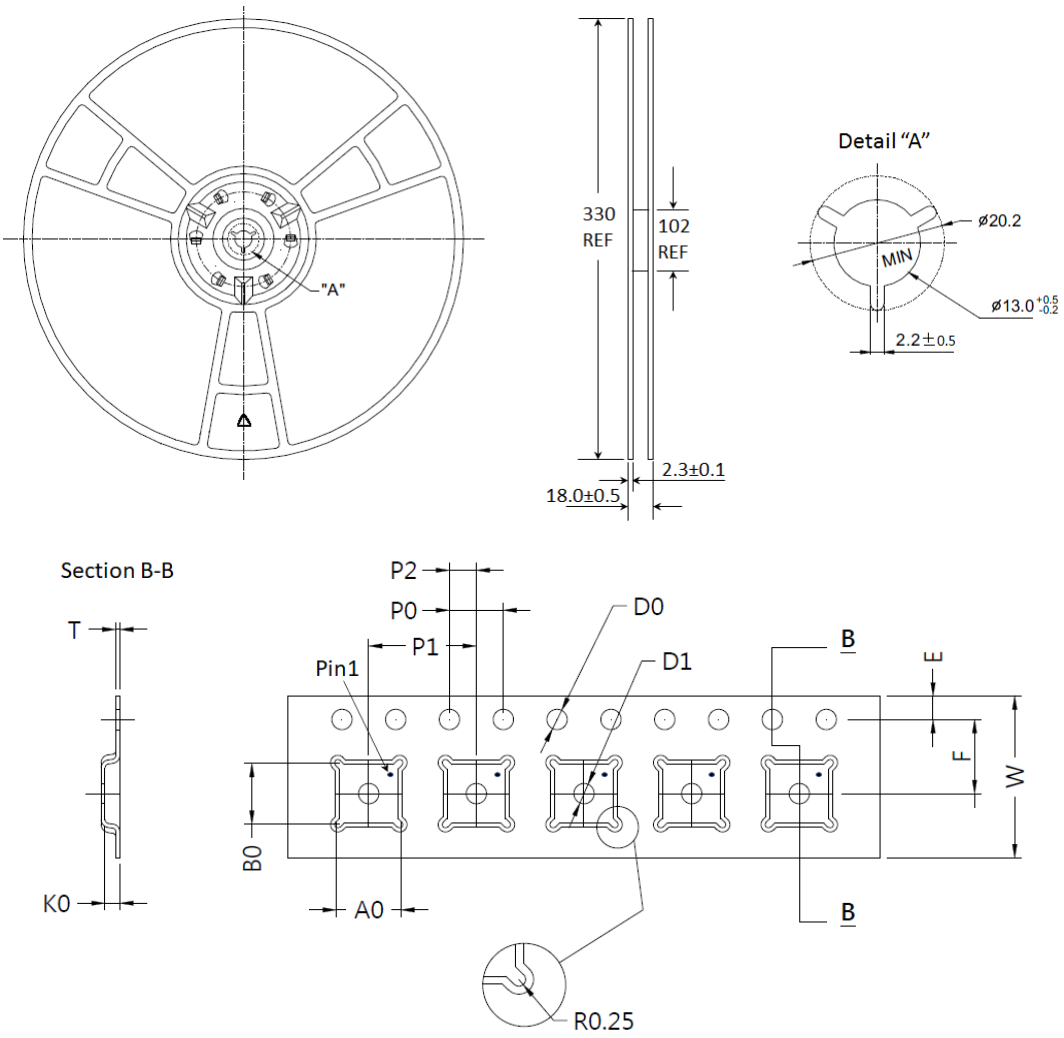


Figure 19: Tape and reel drawing.

Table 16: Tape and Reel Dimensions

Dimension	Value [mm]	Tolerance [mm]	Dimension	Value [mm]	Tolerance [mm]
A0	6.35	±0.10	K0	1.10	±0.10
B0	6.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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Glossary

LNA	Low noise amplifier
NF	Noise figure
OP1dB	Output power at 1 dB gain compression
OIP3	Output third-order intercept point
IL	Insertion loss
IRL, ORL	Input return loss, output return loss
Mu1	Stability factor μ
HG, LG	High gain mode, low gain mode
BP	Bypass (second LNA stage)
PD	Power-down
ANT	Antenna port (RF input)
RXOUT	Receiver output
TERM	Termination output, transmitter path
NIC	Not internally connected
EVB	Evaluation board
LTE	Long Term Evolution
PAR	Peak to average ratio
ENR	Excess noise ratio
SDARS	Satellite digital audio radio service

Changelog

Table 17: Changelog

Date	Revision	Notes
07/30/2024	2.6	Word datasheet (file name Rev 2.7).
11/05/2026	3.00	Discontinued. Transferred to the TagoreTech datasheet format for archiving; content, plots and graphics are unchanged from the Word datasheet revision 2.6. Typographical corrections only: return loss unit dB, EVB B frequency range in the table title, BOM quantities and one manufacturer name, J8 description, test procedure part number and references. Links to application notes TN-001/TN-002, QR code link to the latest datasheet, glossary.

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Discontinued product

The TSL8329M is discontinued. No alternative part is available. Only very few samples are available; please contact TagoreTech: support@tagoretech.com.

TSL8329M Product Information

Latest version of TSL8329M datasheet (archive) is available for download: TSL8329M Datasheet

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